

Cmd	Meaning	Inherent	Immediate	Direct	Extended	Indx/Indir	Relative	H N Z V C
ABX	Add B to X	\$3A (3/1)						-----
ADCA	Add with Carry to A		\$89 (2/2)	\$99 (4/2)	\$B9 (5/3)	\$A9 (4+/2+)		8****
ADCB	Add with Carry to B		\$C9 (2/2)	\$D9 (4/2)	\$F9 (5/3)	\$E9 (4+/2+)		8****
ADDA	Add to A		\$8B (2/2)	\$9B (4/2)	\$BB (5/3)	\$AB (4+/2+)		8****
ADDB	Add to B		\$CB (2/2)	\$DB (4/2)	\$FB (5/3)	\$EB (4+/2+)		8****
ADDD	add to AB (16 bit)		\$C3 (4/3)	\$D3 (6/2)	\$F3 (7/3)	\$E3 (6+/2+)		8****
ANDA	And with A		\$84 (2/2)	\$94 (4/2)	\$B4 (5/3)	\$A4 (4+/2+)		---*0-
ANDB	And with B		\$C4 (2/2)	\$D4 (4/2)	\$F4 (5/3)	\$E4 (4+/2+)		---*0-
ANDCC	And with ConditionCode		\$1C (3/2)					---*7
ASL	Arithmetic Shift Left			\$08 (6/2)	\$78 (7/3)	\$68 (6+/2+)		8****
ASLA	Arithmetic Shift Left A	\$48 (2/1)						8****
ASLB	Arithmetic Shift Left B	\$58 (2/1)						8****
ASR	Arithmetic Shift Right			\$07 (6/2)	\$77 (7/3)	\$67 (6+/2+)		8****
ASRA	Arithmetic Shift Right A	\$47 (2/1)						8****
ASRB	Arithmetic Shift Right B	\$46 (2/1)						8****
BCC	Branch if Carry Clear C=0						\$24 (3/2)	-----
BCS	Branch if Carry Set C=1						\$25 (3/2)	-----
BEQ	Branch if Equal Z=1						\$27 (3/2)	-----
BGE	Branch if Greater than or equal to zero						\$2C (3/2)	-----
BGT	Branch if Greater than Zero						\$2E (3/2)	-----
BHI	Branch if Higher Z+C=0						\$22 (3/2)	-----
BHS	Branch if Higher or Same C=0						\$24 (3/2)	-----
BITA	Bit Test A		\$85 (2/2)	\$95 (4/2)	\$B5 (5/3)	\$A5 (4+/2+)		8***0
BITB	Bit Test B		\$C5 (2/2)	\$D5 (4/2)	\$F5 (5/3)	\$E5 (4+/2+)		8***0
BLE	Branch if Less than or Equal to Zero						\$2F (3/2)	-----
BLO	Branch if Lower C=1						\$25 (3/2)	-----
BLS	Branch if Lower or Same C+Z=1						\$23 (3/2)	-----
BLT	Branch if Less Than Zero						\$2D (3/2)	-----
BMI	Branch if Minus N=1						\$2B (3/2)	-----
BNE	Branch if Not Equal to Zero Z=0						\$26 (3/2)	-----
BPL	Branch if Plus N=0						\$2A (3/2)	-----
BRA	Branch Always						\$20 (3/2)	-----
BRN	Branch Never						\$21 (3/2)	-----
BSR	Branch to Subroutine						\$8D (3/2)	-----
BVC	Branch if Overflow Clear V=0						\$28 (3/2)	-----
BVS	Branch if Overflow Set V=1						\$29 (3/2)	-----
CLR	Clear			\$0F (6/2)	\$7F (7/3)	\$6F (6+/2+)		-0 1 0 0
CLRA	Clear A	\$4F (2/1)						-0 1 0 0
CLRB	Clear B	\$5F (2/1)						-0 1 0 0
CMFA	Compare with A		\$81 (2/2)	\$91 (4/2)	\$B1 (5/3)	\$A1 (4+/2+)		8****
CMFB	Compare with B		\$C1 (2/2)	\$D1 (4/2)	\$F1 (5/3)	\$E1 (4+/2+)		8****
CMFD	Compare with AB		\$10 83 (5/4)	\$10 93 (7/3)	\$10 B3 (8/4)	\$10 A3 (7+/3+)		8****
CMFS	Compare with S		\$11 8C (5/4)	\$11 9C (7/3)	\$11 BC (8/4)	\$11 AC (7+/3+)		8****
CMFU	Compare with U		\$11 83 (5/4)	\$11 93 (7/3)	\$11 B3 (8/4)	\$11 A3 (7+/3+)		8****
CMFX	Compare with X		\$8C (4/3)	\$9C (6/2)	\$BC (7/3)	\$AC (6+/2+)		8****
CMFY	Compare with Y		\$10 8C (5/4)	\$10 9C (7/3)	\$10 BC (8/4)	\$10 AC (7+/3+)		8****
COM	Complement			\$03 (6/2)	\$73 (7/3)	\$63 (6/2)		---*0 1
COMA	Complement A	\$43 (2/1)						---*0 1
COMB	Complement B	\$53 (2/1)						---*0 1
CWAI	And with CC and Wait		\$3C (20/2)					---*7
DAA	Decimal Adjust after Addition	\$19 (2/1)						---*0
DEC	Decrement			\$0A (6/2)	\$7A (7/3)	\$6A (6+/2+)		8****
DECA	Decrement A	\$4A (2/1)						8****
DECB	Decrement B	\$5A (2/1)						8****
EXORA	Exclusive Or A (Xor)		\$88 (2/2)	\$98 (4/2)	\$B8 (5/3)	\$A8 (4+/2+)		---*0-
EXORB	Exclusive Or B (Xor)		\$C8 (2/2)	\$D8 (4/2)	\$F8 (5/3)	\$E8 (4+/2+)		---*0-
EXG	Exchange Register Contents		\$1E (8/2)					-----
INC	Increment			\$0C (6/2)	\$7C (7/3)	\$6C (6+/2+)		8****
INCA	Increment A	\$4C (2/1)						8****
INCB	Increment B	\$5C (2/1)						8****
JMP	Jump			\$0E (3/2)	\$7E (4/3)	\$6E (3+/2+)		-----
JSR	Jump to Subroutine			\$9D (7/2)	\$8D (8/3)	\$AD (7+/2+)		-----
LBCC	Long Branch if Carry Clear C=0						\$10 24 (5+/4)	-----
LBCCS	Long Branch if Carry Set C=1						\$10 25 (5+/4)	-----
LBCCQ	Long Branch if Equal Z=1						\$10 27 (5+/4)	-----
LBCCGE	Long Branch if Greater than or equal to zero						\$10 2C (5+/4)	-----
LBCCGT	Long Branch if Greater than Zero						\$10 2E (5+/4)	-----
LBCCI	Long Branch if Higher Z+C=0						\$10 22 (5+/4)	-----
LBCCHS	Long Branch if Higher or Same C=0						\$10 24 (5+/4)	-----
LBCCBLE	Long Branch if Less than or Equal to Zero						\$10 2F (5+/4)	-----
LBCCLO	Long Branch if Lower C=1						\$10 25 (5+/4)	-----
LBCCLS	Long Branch if Lower or Same C+Z=1						\$10 23 (5+/4)	-----
LBCCLT	Long Branch if Less Than Zero						\$10 2D (5+/4)	-----
LBCCMI	Long Branch if Minus N=1						\$10 2B (5+/4)	-----
LBCCNE	Long Branch if Not Equal to Zero Z=0						\$10 28 (5+/4)	-----
LBCCPL	Long Branch if Plus N=0						\$10 2A (5+/4)	-----
LBCCRA	Long Branch Always						\$16 (5/3)	-----
LBCCRN	Long Branch Never						\$10 21 (5/4)	-----
LBCCSR	Long Branch to Subroutine						\$17 (9/3)	-----
LBCCVVC	Long Branch if Overflow Clear V=0						\$10 28 (5+/6)	-----
LBCCVVS	Long Branch if Overflow Set V=1						\$10 29 (5+/6)	-----
LDA	Load A		\$86 (2/2)	\$96 (4/2)	\$B6 (5/3)	\$A6 (4+/2+)		---*0-
LDB	Load B		\$C6 (2/2)	\$D6 (4/2)	\$F6 (5/3)	\$E6 (4+/2+)		---*0-
LDD	Load AB		\$CC (3/3)	\$DC (5/2)	\$FC (6/3)	\$EC (5+/2+)		---*0-
LDS	Load S		\$10 CE (4/4)	\$10 DE (6/3)	\$10 FE (7/4)	\$10 EE (6+/3+)		---*0-
LDU	Load U		\$CE (3/3)	\$DE (5/2)	\$FE (6/3)	\$EE (5+/2+)		---*0-
LDX	Load X		\$8E (3/3)	\$9E (5/2)	\$BE (6/3)	\$AE (5+/2+)		---*0-
LDY	Load Y		\$10 8E (4/4)	\$10 9E (6/3)	\$10 BE (7/4)	\$10 AE (6+/3+)		---*0-
LEAS	Load Effective Address into S						\$32 (4+/2+)	-----
LEAU	Load Effective address into U						\$33 (4+/2+)	-----
LEAX	Load Effective Address into X						\$30 (4+/2+)	-----
LEAY	Load Effective Address into Y						\$31 (4+/2+)	-----
LSL	Logical Shift Left			\$08 (6/2)	\$78 (7/3)	\$68 (6+/2+)		8****
LSLA	Logical Shift Left A	\$48 (2/1)						8****
LSLB	Logical Shift Left B	\$58 (2/1)						8****
LSR	Logical Shift Right			\$04 (6/2)	\$74 (7/3)	\$64 (6+/2+)		-0 * *
LSRA	Logical Shift Right A	\$44 (2/1)						-0 * *
LSRB	Logical Shift Right B	\$54 (2/1)						-0 * *
MUL	Multiply A*B - result in AB	\$3D (11/1)						---*9
NEG	Negate			\$00 (6/2)	\$70 (7/3)	\$60 (6+/2+)		8****
NEGA	Negate A	\$40 (2/1)						8****
NEGB	Negate B	\$50 (2/1)						8****
NOP	No Operation	\$12 21						-----
ORA	Or A		\$8A (2/2)	\$9A (4/2)	\$BA (5/3)	\$AA (4+/2+)		---*0-
ORB	Or B		\$CA (2/2)	\$DA (4/2)	\$FA (5/3)	\$EA (4+/2+)		---*0-
ORCC	Or Condition Code		\$1A (3/2)					---*7
PSHS	Push onto S stack (PC U Y X DP B A CC)		\$34 (3/2)					-----
PSHU	Push onto U stack (PC S Y X DP B A CC)		\$36 (3/2)					-----
PULS	Pull off S stack (PC U Y X DP B A CC)		\$35 (3/2)					-----
PULU	Pull off U stack (PC S Y X DP B A CC)		\$37 (3/2)					-----
ROL	Rotate Left through Carry			\$09 (6/2)	\$79 (7/3)	\$69 (6+/2+)		8****
ROLA	Rotate Left through Carry A	\$49 (2/1)						8****
ROLB	Rotate Left through Carry B	\$59 (2/1)						8****
ROR	Rotate Right through Carry			\$06 (6/2)	\$76 (7/3)	\$66 (6+/2+)		8****
RORA	Rotate Right through Carry A	\$46 (2/1)						8****
RORB	Rotate Right through Carry B	\$56 (2/1)						8****
RTI	Return from Interrupt	\$3B (6/15)						---*7
RTS	Return from Subroutine	\$39 (5/1)						-----
SBCA	Subtract with Carry from A		\$82 (2/2)	\$92 (4/2)	\$B2 (5/3)	\$A2 (4+/2+)		8****
SBCB	Subtract with Carry from B		\$C2 (2/2)	\$D2 (4/2)	\$F2 (5/3)	\$E2 (4+/2+)		8****
SEX	Sign Extend B into AB	\$1D (2/1)						---*0-
STA	Store A			\$97 (4/2)	\$B7 (5/3)	\$A7 (4+/2+)		---*0-
STB	Store B			\$D7 (4/2)	\$F7 (5/3)	\$E7 (4+/2+)		---*0-
STD	Store AB			\$DD (5/2)	\$FD (6/3)	\$ED (5+/2+)		---*0-
STS	Store S			\$10 DF (6/3)	\$10 FF (7/4)	\$10 EF (6+/3+)		---*0-
STU	Store U			\$DF (5/2)	\$FF (6/3)	\$EF (5+/2+)		---*0-
STX	Store X			\$9F (5/2)	\$BF (6/3)	\$AF (5+/2+)		---*0-
STY	Store Y			\$10 9F (6/3)	\$10 BF (7/4)	\$10 AF (6+/3+)		---*0-
SUBA	Subtract from A		\$80 (2/2)	\$90 (4/2)	\$B0 (5/3)	\$A0 (4+/2+)		8****
SUBB	Subtract from B		\$C0 (2/2)	\$D0 (4/2)	\$F0 (5/3)	\$E0 (4+/2+)		8****
SUBD	Subtract from AB		\$83 (4/3)	\$93 (6/2)	\$B3 (7/3)	\$A3 (6+/2+)		8****
SWI	Software Interrupt	\$3F (19/1)						-----
SWI2	Software Interrupt 2	\$10 3F (20/2)						-----
SWI3	Software Interrupt 3	\$11 3F (20/2)						-----
SYNC	Synchronise to Ext Event (wait for interrupt)	\$13 (2/1)						-----
TFR	Transfer Register to Register (X,Y,U,S,A,B,D,PC,CC)		\$1F (7/2)					-----
TST	Test			\$0D (6/2)	\$7D (7/3)	\$6D (6+/2+)		---*0-
TSTA	Test A	\$4D (2/1)						---*0-
TSTB	Test B	\$5D (2/1)						---*0-

Cmd	Meaning	Inherent	Immediate	Direct	Extended	Indx/Indir	Relative	E F H I N Z V C
ADCD	Add Memory Word plus Carry with Accumulator D		\$18 09 (4/4-5)	\$10 99 (3/5-7)	\$10 B9 (6-8)	\$10 A9 (6-7/3)	*
ADCR	Add Source Register plus Carry to Destination Register		\$10 31 (3/4)				*
ADDE	Add Memory Byte to 8-Bit Accumulator E		\$11 8B (3/3)	\$11 9B (4/5/3)	\$11 BB (3+/5+)	\$11 AB (3+/5+)	*
ADDF	Add Memory Byte to 8-Bit Accumulator F		\$11 CB (3/3)	\$11 DB (5/4)	\$11 FB (4/5-6)	\$11 EB (3+/5+)	*
ADWW	Add Memory Word to 16-Bit Accumulator W		\$10 8B (4/4-5)	\$10 9B (3/5-7)	\$10 BB (4/6-8)	\$10 AB (3+/6+)	*
ADDR	Add Source Register to Destination Register		\$10 30 (3/4)				*
AIM	Logical AND of Immediate Value with Memory Byte			\$02 (3/6)	\$72 (4/7)	\$62 (3+/7+)	* 0
ANDD	Logically AND Memory Word with Accumulator D		\$10 84 (4/4-5)	\$10 94 (3/5-7)	\$10 B4 (4/6-8)	\$10 A4 (3+/6+)	* 0
ANDR	Logically AND Source Register with Destination Register		\$10 34 (3/4)				* 0
ASLD	Arithmetic Shift Left of Accumulator D	\$10 84 (2/2-3)					**
ASRD	Arithmetic Shift Right of Accumulator D	\$10 3F (2/2-3)					**
BAND	Logically AND Register Bit with Memory Bit			\$11 30 (4/6-7)			**
BEOR	Exclusive-OR Register Bit with Memory Bit			\$11 34 (4/6-7)			**
BIEOR	Exclusively-OR Register Bit with Inverted Memory Bit			\$11 35 (4/6-7)			**
BIOR	Logically OR Register Bit with Inverted Memory Bit			\$11 33 (4/6-7)			**
BITD	Bit Test Accumulator D with Memory Word Value		\$10 85 (4/4-5)	\$10 95 (3/5-7)	\$10 B5 (4/6-8)	\$10 A5 (3+/6+)	* 0
BITMD	Bit Test the MD Register with an Immediate Value		\$11 3C (3/4)				**
BOR	Logically OR Memory Bit with Register Bit			\$11 32 (4/6-7)			**
CLRD	Load Zero into Accumulator		\$10 4F (2/2-3)				- 0 1 0 0
CLRE	Load Zero into Accumulator		\$11 4F (2/2-3)				- 0 1 0 0
CLRF	Load Zero into Accumulator		\$11 5F (2/2-3)				- 0 1 0 0
CLRW	Load Zero into Accumulator		\$10 5F (2/2-3)				- 0 1 0 0
CMPE	Compare Memory Byte from 8-Bit Accumulator		\$11 81 (3/3)	\$11 91 (3/4-5)	\$11 B1 (3/5-6)	\$11 A1 (3/4-5)	**
CMPE	Compare Memory Byte from 8-Bit Accumulator		\$11 C1 (3/3)	\$11 D1 (3/4-5)	\$11 F1 (3/5-6)	\$11 E1 (3/4-5)	**
CMFW	Compare Memory Word from 16-Bit Register		\$10 81 (4/4-5)	\$10 91 (3/5-7)	\$10 B1 (4/6-8)	\$10 A1 (3+/6+)	**
CMFR	Compare Source Register from Destination Register		\$10 37 (3/4)				**
COMD	Complement Accumulator		\$10 43 (2/2-3)				* 0 1
COME	Complement Accumulator		\$11 43 (2/2-3)				* 0 1
COMF	Complement Accumulator		\$11 53 (2/2-3)				* 0 1
COMW	Complement Accumulator		\$10 43 (2/2-3)				* 0 1
DECD	Decrement Accumulator		\$10 4A (2/2-3)				**
DECE	Decrement Accumulator		\$11 4A (2/2-3)				**
DECF	Decrement Accumulator		\$11 5A (2/2-3)				**
DECW	Decrement Accumulator		\$10 4A (2/2-3)				**
DIVD	Signed Divide of Accumulator D by 8-bit value in Memory		\$11 8D (3/25)	\$11 9D (3/26-27)	\$11 BD (4/27-28)	\$11 AD (3+/27+)	**
DIVQ	Signed Divide of Accumulator Q by 16-bit value in Memory		\$11 8E (4/34)	\$11 9E (3/25-36)	\$11 BE (4/36-37)	\$11 AE (3/36+)	**
EIM	Exclusive-OR of Immediate Value with Memory Byte			\$05 (3/6)	\$65 (3+/7+)	\$75 (4/7)	* 0
EORR	Exclusively-OR Memory Word with Accumulator D		\$10 88 (4/4-5)	\$10 98 (3/5-7)	\$10 B8 (4/6-8)		* 0
EORR	Exclusively-OR Source Register with Destination Register		\$10 36 (3/4)				* 0
INCD	Increment Accumulator		\$10 4C (2/2-3)				**
INCE	Increment Accumulator		\$11 4C (2/2-3)				**
INCF	Increment Accumulator		\$11 5C (2/2-3)				**
INCW	Increment Accumulator		\$10 5C (2/2-3)				**
LDE	Load Data into 8-Bit Accumulator		\$11 86 (3/3)	\$11 96 (3/3)	\$11 B6 (3/3)	\$11 A6 (3/3)	* 0
LDF	Load Data into 8-Bit Accumulator		\$11 C6 (3/3)	\$11 D6 (3/3)	\$11 F6 (3/3)	\$11 E6 (3/3)	* 0
LDW	Load Data into 16-Bit Register		\$10 86 (4/4)	\$10 96 (3/5-6)	\$10 B6 (4/6-7)	\$10 A6 (3+/6+)	* 0
LDBT	Load Memory Bit into Register Bit			\$11 36 (4/6-7)			**
LDMD	Load an Immediate Value into the MD Register		\$11 3D (3/5)				**
LDD	Load 32-bit Data into Accumulator Q		\$CD (5/5)	\$10 DC (3/7-8)	\$10 FC (4/8-9)	\$10 EC (3+/8+)	* 0
LSL D	Logical Shift Left of Accumulator D	\$10 48 (2/2-3)					**
LSR D	Logical Shift Right of 16-Bit Accumulator	\$10 44 (2/2-3)					- 0 * **
LSR W	Logical Shift Right of 16-Bit Accumulator	\$10 54 (2/2-3)					- 0 * **
MULD	Signed Multiply of Accumulator D and Memory Word		\$11 8F (4/28)	\$11 9F (3/29-30)	\$11 BF (4/30-31)	\$11 AF (3+/30+)	**
NEGD	Negation (Twos-Complement) of Accumulator	\$10 40 (2/2-3)					**
OIM	Logical OR of Immediate Value with Memory Byte			\$01 (3/6)	\$71 (4/7)	\$61 (3+/7+)	* 0
ORD	Logically OR Accumulator D with Word from Memory		\$10 8A (4/4-5)	\$10 9A (3/5-7)	\$10 BA (4/6-8)	\$10 AA (3+/6+)	* 0
ORR	Logically OR Source Register with Destination Register		\$10 35 (3/4)				* 0
PSHSW	Push Accumulator W onto the Hardware Stack	\$10 38 (2/6)					**
PSHUW	Push Accumulator W onto the User Stack	\$10 3A (2/6)					**
PULSW	Pull Accumulator W from the Hardware Stack	\$10 39 (2/6)					**
PULUW	Pull Accumulator W from the User Stack	\$10 3B (2/6)					**
ROL D	Rotate 16-Bit Accumulator Left through Carry	\$10 49 (2/2-3)					**
ROL W	Rotate 16-Bit Accumulator Left through Carry	\$10 59 (2/2-3)					**
ROR D	Rotate 16-Bit Accumulator Right through Carry	\$10 46 (2/2-3)					**
ROR W	Rotate 16-Bit Accumulator Right through Carry	\$10 56 (2/2-3)					**
SBCD	Subtract Memory Word and Carry from Accumulator D		\$10 82 (4/4-5)	\$10 92 (3/5-7)	\$10 B2 (3+/6+)	\$10 A2 (3+/6+)	**
SBCR	Subtract Source Register and Carry from Destination Register		\$10 33 (3/4)				**
SEXW	Sign Extend a 16-bit Value in W to a 32-bit Value in Q	\$14 (1/4)					**
STE	Store 8-Bit Accumulator to Memory			\$11 97 (3/4-5)	\$11 B7 (4/5-6)	\$11 A7 (3+/5+)	* 0
STF	Store 8-Bit Accumulator to Memory			\$11 D7 (3/4-5)	\$11 F7 (4/5-6)	\$11 E7 (3+/5+)	* 0
STW	Store 16-Bit Register to Memory			\$10 97 (3/5-6)	\$10 B7 (4/6-7)	\$10 A7 (3+/6+)	* 0
STBT	Store value of a Register Bit into Memory			\$11 37 (4/7-8)			**
STQ	Store Contents of Accumulator Q to Memory			\$10 DD (3/7-8)	\$10 FD (4/8-9)	\$10 ED (3+/8+)	* 0
SUBE	Subtract from value in 8-Bit Accumulator		\$11 80 (3/3)	\$11 90 (3/4-5)	\$11 B0 (4/5-6)	\$11 A0 (4/5-6)	**
SUBF	Subtract from value in 8-Bit Accumulator		\$11 C0 (3/3)	\$11 D0 (3/4-5)	\$11 F0 (4/5-6)	\$11 E0 (4/5-6)	**
SUBW	Subtract from value in 16-Bit Accumulator		\$10 80 (4/4-5)	\$10 90 (3/5-7)	\$10 B0 (4/6-8)	\$10 A0 (3+/6+)	**
SUBR	Subtract Source Register from Destination Register		\$10 32 (3/4)				**
TFM ++	Transfer Memory		\$11 38 (3/9+)				**
TFM --	Transfer Memory		\$11 39 (3/9+)				**
TFM +x	Transfer Memory		\$11 3A (3/9+)				**
TFM +x*	Transfer Memory		\$11 3B (3/9+)				**
TIM	Bit Test Immediate Value with Memory Byte			\$0B (3/6)	\$7B (4/7)	\$6B (3+/7+)	* 0
TSTD	Test Value in Accumulator	\$10 4D (2/2-3)					* 0
TSTE	Test Value in Accumulator	\$11 4D (2/2-3)					* 0
TSTF	Test Value in Accumulator	\$11 5D (2/2-3)					* 0
TSTW	Test Value in Accumulator	\$10 5D (2/2-3)					* 0