		Implied	Relative	Accumulator	Immediate	Zero Page	Zero Page,X	Zero Page,Y	Absolute	Absolute,X	Absolute,Y	Indirect	(Indirect,X)	(Indirect),Y	C Z I D B V N
		no params	jr	works on A	#nn &nn	$nn (&00nn)	$nn,X (&00nn+X)	$nn,Y (&00nn+Y)	$0100 (&0100)	$0100,X (&0100+X)	$0100,Y (&0100+Y)	($nnnn) ((&nnnn))	($nn,X) ((&00nn+X))	($nn),Y ((&00nn)+Y)	
ADC	Add with Carry				$69 2 2	$65 2 3	$75 2 4		$6D 3 4	$7D 3 4/5	$79 3 4/5	$72 3	$61 2 6	$71 2 5/6	Ovf7 Z - - - +- 7
AND	Logical AND				$29 2 2	$25 2 3	$35 2 4		$2D 3 4	$3D 3 4/5	$39 3 4/5	$32 3	$21 2 6	$31 2 5/6	- Z - - - - 7
ASL	Arithmetic Shift Left (SLA)			$0A 1 2		$06 2 5	$16 2 6		$0E 3 6	$1E 3 7					7 Z - - - - 7
BCC	Branch if Carry Clear C=1 (JP C,)		$90 2 2/3/4												- - - - - - -
BCS	Branch if Carry Set C=0 (JP NC,)		$B0 2 2/3/4												- - - - - - -
BEQ	Branch if Equal to Zero (Z = 1 JP Z,)		$F0 2 2/3/4												- - - - - - -
BIT	Bit Test (And A with mem loc)				$89 2	$24 2 3	$34 2		$2C 3 4	$3C 3					- Z - - - 6 7
BMI	Branch if Minus (S = 1)		$30 2 2/3/4												- - - - - - -
BNE	Branch if Not Equal to Zero (Z = 0 JP NZ,)		$D0 2 2/3/4												- - - - - - -
BPL	Branch if Plus (S = 0)		$10 2 2/3/4												- - - - - - -
BRK	Break	$00 1 7													- - - - =1 - -
BVC	Branch if Overflow Clear		$50 2 2/3/4												- - - - - - -
BVS	Branch if Overflow Set		$70 2 2/3/4												- - - - - - -
CLC	Clear Carry Flag														=0 - - - - - -
CLD	Clear Decimal Mode	$D8 1 2													- - - =0 - - -
CLI	Clear Interrupt Mask (EI)	$58 1 2													- - =0 - - - -
CLV	Clear Overflow Flag	$B8 1 2													- - - - - =0 -
CMP	Compare Accumulator to Memory				$C9 2 2	$C5 2 3	$D5 2 4		$CD 3 4	$DD 3 4/5	$D9 3 4/5	$D2 3	$C1 2 6	$D1 2 5/6	> = - - - - 7
CPX	Compare with Index Register X				$E0 2 2	$E4 2 3			$EC 3 4						> = - - - - 7
CPY	Compare with Index Register Y				$C0 2 2	$C4 2 3			$CC 3 4						> = - - - - 7
DEC	Decrement			$3A (or DEA)		$C6 2 5	$D6 2 6		$CE 3 6	$DE 3 7					- Z - - - - 7
DEX	Decrement Index Register X	$CA 1 2													- Z - - - - 7
DEY	Decrement Index Register Y	$88 1 2													- Z - - - - 7
EOR	Logical Exclusive-OR (XOR)	$49 2 2				$45 2 3	$55 2 4		$4D 3 4	$5D 3 4/5	$59 3/4/5	$52 3	$41 2 6	$51 2 5/6	- Z - - - - 7
INC	Increment			$1A (or INA)		$E6 2 5	$F6 2 6		$EE 3 6	$FE 3 7					- Z - - - - 7
INX	Increment Index Register X	$E8 1 2													- Z - - - - 7
INY	Increment Index Register Y	$C8 1 2													- Z - - - - 7
JMP	Jump to New Location								$4C 3 3	$7C 3		$6C 3 5			- - - - - - -
JSR	Jump to Subroutine								$20 3 6						- - - - - - -
LDA	Load Accumulator				$A9 2 2	$A5 2 3	$B5 2 4		$AD 3 4	$BD 3 4/5	$B9 3 4/5	$B2 3	$A1 2 6	$B1 2 5	- Z - - - - 7
LDX	Load Index Register X				$A2 2 2	$A6 2 3		$B6 2 4	$AE 3 4		$BE 3 4/5				- Z - - - - 7
LDY	Load Index Register Y				$A0 2 2	$A4 2 3	$B4 2 4		$AC 3 4	$BC 3 4/5					- Z - - - - 7
LSR	Logical Shift Right (BitShift Right topbit 0)			$4A 1 2		$46 2 5	$56 2 6		$4E 3 6	$5E 3 7					- Z - - - - 7
NOP	No Operation	$EA 1 2													- - - - - - -
ORA	Logical (Inclusive) OR				$09 2 2	$05 2 3	$15 2 4		$0D 3 4	$1D 3 4/5	$19 3 4/5	$12 3	$01 2 6	$11 2 5/6	- Z - - - - 7
PHA	Push Accumulator onto Stack (PUSH A)	$48 1 3													- - - - - - -
PHP	Push Processor Status (PUSH F)	$08 1 3													- - - - - - -
PLA	Pull Accumulator from Stack (POP A)	$68 1 4													- Z - - - - 7
PLP	Pull Processor Status (POP F)	$28 1 4													S S S S S S S
ROL	Rotate Left through Carry (RLCA)			$2A 1 2		$26 2 5	$36 2 6		$2E 3 6	$3E 3 7					old7 Z - - - - 7
ROR	Rotate Right through Carry			$6A 1 2		$66 2 5	$76 2 6		$6E 3 6	$7E 3 7					old0 Z - - - - 7
RTI	Return from Interrupt (RETI)	$40 1 6													S S S S S S S
RTS	Return from Subroutine (RET)	$60 1 6													- - - - - - -
SBC	Subtract with Carry				$E9 2 2	$E5 2 3			$ED 3 4	$FD 3 4/5	$F9 3 4/5	$F2 3	$E1 2 6	$F1 2 5/6	Ovf7 Z - - - - 7
SEC	Set Carry (SCF)	$38 1 2													1 - - - - - -
SED	Set Decimal Flag	$F8 1 2													- - - 1 - - -
SEI	Set Interrupt Mask (Disable Interrupts)	$78 1 2													- - 1 - - - -
STA	Store Accumulator					$85 2 3	$95 2 4		$8D 3 4	$9D 3 5	$99 3 5	$92 3	$81 2 6	$91 2 6	- - - - - - -
STX	Store Index Register X					$86 2 3		$96 2 4	$8E 3 4						- - - - - - -
STY	Store Index Register Y					$84 2 3	$94 2 4		$8C 3 4						- - - - - - -
TAX	Transfer Accumulator to Index Register X	$AA 1 2													- Z - - - - 7
TAY	Transfer Accumulator to Index Register Y	$A8 1 2													- Z - - - - 7
TSX	Transfer Stack Pointer to X (LD X,SP)	$BA 1 2													- Z - - - - 7
TXA	Transfer Index Register X to Accumulator	$8A 1 2													- Z - - - - 7
TXS	Transfer X to Stack Pointer (LD SP,X)	$9A 1 2													- - - - - - -
TYA	Transfer Index Register Y to Accumulator	$98 1 2													- Z - - - - 7
BBR	Branch if bit n is Reset (also some 65c02)					$0f-$7F 2									
BBS	Branch if bit n is Set (also some 65c02)					$8f-$FF 2									
BRA	Branch Relative Always (JR)		$80 2												
BSR	Branch to subroutine (Call Relative)	$44 2 8													
CLX	Clear X	$82 1 2													
CLY	Clear Y	$C2 1 2													
CSH	Change Speed High (7.16 MHz)	$D4 1 3													
CSL	Change Speed Low (1.78 MHz)	$54 1 3													
PHX	Push X	$DA 1													
PLX	Pull X	$FA 1													
PHY	Push Y	$5A 1													
PLY	Pull Y	$7A 1													
RMB	Reset Memory Bit n (also some 65c02)					$07-$77									
SAX	Swap A and X	$22 1 3													
SAY	Swap A and Y	$42 1 3													
SET	Set T flag (works on ADC, AND, EOR, ORA,SBC)	$F4 1 2													
SMB	Set Memory Bit n (also some 65c02)					$87-$F7									
ST0	ST0 - Store (HuC6270) VDC No. 0				$03 2 5										
ST1	ST1 - Store (HuC6270) VDC No. 1				$13 2 5										
ST2	ST2 - Store (HuC6270) VDC No. 2				$23 2 5										
STP	Stop processor until next RST (HALT – not	$D8 1													
STZ	Store Zero to address					$64 2	$74 2		$9C 3	$9E 3					
SXY	Swap X and Y registers	$02 1 3													
TAI	Transfer Alternate Increment				$F3 7 17+										
TAM	Tranfer Accumulator to MPR				$53 2 5										
TIA	Transfer Increment Alternate				$E3 7 17+										
TII	Transfer Increment Increment				$73 7 17+										
TIN	Transfer Increment				$D3 7 17+										
TMA	Tranfer MPR to Accumulator				$43 2 4										
TRB	Test and Reset Bits with A					$14 2			$1C 3						
TSB	Test and Set Bits with A					$04 2			$0C 3						
TST	Test Bits at n2 witn n1					$83 3 7	$A3 3 7	$93 4 8	$B3 4 8						

Black:6502 Red:HuC6280 Green:65C02/HCU6280