

# Opcode Matrix

MSD	LSD																MSD
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	BRK s 2 7	ORA (d,x) 2 6	COP s 2 7	ORA d,s 2 4	TSB d 2 5	ORA d 2 3	ASL d 2 5	ORA [d] 2 6	PHP s 1 3	ORA # 2 2	ASL A 1 2	PHD s 1 4	TSB a 3 6	ORA a 3 4	ASL a 3 6	ORA al 4 5	0
1	BPL r 2 2	ORA (d,y) 2 5	ORA (d) 2 5	ORA (d,s,y) 2 7	TRB d 2 5	ORA d,x 2 4	ASL d,x 2 6	ORA [d],y 2 6	CLC i 1 2	ORA a,y 3 4	INC A 1 2	TCS i 1 2	TRB a 3 6	ORA a,x 3 4	ASL a,x 3 7	ORA al,x 4 5	1
2	JSR a 3 6	AND (d,x) 2 6	JSL al 4 8	AND d,s 2 4	BIT d 2 3	AND d 2 3	ROL d 2 5	AND [d] 2 6	PLP s 1 4	AND # 2 2	ROL A 1 2	PLD s 1 5	BIT a 3 4	AND a 3 4	ROL a 3 6	AND al 4 5	2
3	BMI r 2 2	AND (d,y) 2 5	AND (d) 2 5	AND (d,s,y) 2 7	BIT d,x 2 4	AND d,x 2 4	ROL d,x 2 6	AND [d],y 2 6	SEC i 1 2	AND a,y 3 4	DEC A 1 2	TSC i 1 2	BIT a,x 3 4	AND a,x 3 4	ROL a,x 3 7	AND al,x 4 5	3
4	RTI s 1 6	EOR (d,x) 2 6	WDM 2 6	EOR d,s 2 4	MVP xyc 3 7	EOR d 2 3	LSR d 2 5	EOR [d] 2 6	PHA s 1 3	EOR # 2 2	LSR A 1 2	PHK s 1 3	JMP a 3 3	EOR a 3 4	LSR a 3 6	EOR al 4 5	4
5	BVC r 2 2	EOR (d,y) 2 5	EOR (d) 2 5	EOR (d,s,y) 2 7	MVN xyc 3 7	EOR d,x 2 4	LSR d,x 2 6	EOR [d],y 2 6	CLI i 1 2	EOR a,y 3 4	PHY s 1 3	TCD i 1 2	JMP al 4 4	EOR a,x 3 4	LSR a,x 3 7	EOR al,x 4 5	5
6	RTS s 1 6	ADC (d,x) 2 6	PER s 3 6	ADC d,s 2 4	STZ d 2 3	ADC d 2 3	ROR d 2 5	ADC [d] 2 6	PLA s 1 4	ADC # 2 2	ROR A 1 2	RTL s 1 6	JMP (a) 3 5	ADC a 3 4	ROR a 3 6	ADC al 4 5	6
7	BVS r 2 2	ADC (d,y) 2 5	ADC (d) 2 5	ADC (d,s,y) 2 7	STZ d,x 2 4	ADC d,x 2 4	ROR d,x 2 6	ADC [d],y 2 6	SEI i 1 2	ADC a,y 3 4	PLY s 1 4	TDC i 1 2	JMP (a,x) 3 6	ADC a,x 3 4	ROR a,x 3 7	ADC al,x 4 5	7
8	BRA r 2 3	STA (d,x) 2 6	BRL rl 3 4	STA d,s 2 4	STY d 2 3	STA d 2 3	STX d 2 3	STA [d] 2 6	DEY i 1 2	BIT # 2 2	TXA i 1 2	PHB s 1 3	STY a 3 4	STA a 3 4	STX a 3 4	STA al 4 5	8
9	BCC r 2 2	STA (d,y) 2 6	STA (d) 2 5	STA (d,s,y) 2 7	STY d,x 2 4	STA d,x 2 4	STX d,y 2 4	STA [d],y 2 6	TYA i 1 2	STA a,y 3 5	TXS i 1 2	TXY i 1 2	STZ a 3 4	STA a,x 3 5	STZ a,x 3 5	STA al,x 4 5	9
A	LDY # 2 2	LDA (d,x) 2 6	LDX # 2 2	LDA d,s 2 4	LDY d 2 3	LDA d 2 3	LDX d 2 3	LDA [d] 2 6	TAY i 1 2	LDA # 2 2	TAX i 1 2	PLB s 1 4	LDY a 3 4	LDA a 3 4	LDX a 3 4	LDA al 4 5	A
B	BCS r 2 2	LDA (d,y) 2 5	LDA (d) 2 5	LDA (d,s,y) 2 7	LDY d,x 2 4	LDA d,x 2 4	LDX d,y 2 4	LDA [d],y 2 6	CLV i 1 2	LDA a,y 3 4	TSX i 1 2	TYX i 1 2	LDY a,x 3 4	LDA a,x 3 4	LDX a,y 3 4	LDA al,x 4 5	B
C	CPY # 2 2	CMP (d,x) 2 6	REP # 2 3	CMP d,s 2 4	CPY d 2 3	CMP d 2 3	DEC d 2 5	CMP [d] 2 6	INY i 1 2	CMP # 2 2	DEX i 1 2	WAI i 1 3	CPY a 3 4	CMP a 3 4	DEC a 3 6	CMP al 4 5	C
D	BNE r 2 2	CMP (d,y) 2 5	CMP (d) 2 5	CMP (d,s,y) 2 7	PEI s 2 6	CMP d,x 2 4	DEC d,x 2 6	CMP [d],y 2 6	CLD i 1 2	CMP a,y 3 4	PHX s 1 3	STP i 1 3	JML (a) 3 6	CMP a,x 3 4	DEC a,x 3 7	CMP al,x 4 5	D
E	CPX # 2 2	SBC (d,x) 2 6	SEP # 2 3	SBC d,s 2 4	CPX d 2 3	SBC d 2 3	INC d 2 5	SBC [d] 2 6	INX i 1 2	SBC # 2 2	NOP i 1 2	XBA i 1 3	CPX a 3 4	SBC a 3 4	INC a 3 6	SBC al 4 5	E
F	BEQ r 2 2	SBC (d,y) 2 5	SBC (d) 2 5	SBC (d,s,y) 2 7	PEA s 3 5	SBC d,x 2 4	INC d,x 2 6	SBC [d],y 2 6	SED i 1 2	SBC a,y 3 4	PLX s 1 4	XCE i 1 2	JSR (a,x) 3 8	SBC a,x 3 4	INC a,x 3 7	SBC al,x 4 5	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

## Op Code Matrix Legend

INSTRUCTION  
MNEMONIC

BASE  
NO. BYTES

★ = New W65C816/802 Opcodes  
● = New W65C02 Opcodes  
Blank = NMOS 6502 Opcodes

ADDRESSING  
MODE

BASE  
NO. CYCLES

symbol	addressing mode	symbol	addressing mode
#	immediate	[d]	direct indirect long
A	accumulator	[d].y	direct indirect long indexed
r	program counter relative	a	absolute
rl	program counter relative long	a,x	absolute indexed (with x)
i	implied	a,y	absolute indexed (with y)
s	stack	al	absolute long
d	direct	al,x	absolute long indexed
d,x	direct indexed (with x)	d,s	stack relative
d,y	direct indexed (with y)	(d,s).y	stack relative indirect indexed
(d)	direct indirect	(a)	absolute indirect
(d,x)	direct indexed indirect	(a,x)	absolute indexed indirect
(d,y)	direct indirect indexed	xy	block move

Opcode			Available on:			# of	# of
Hex	Mnemonic	Addressing Mode	6502	65C02	65802/816	Bytes	Cycles
00	BRK	Stack/Interrupt	x	x	x	2**	7 <sup>9</sup>
01	ORA	DP Indexed Indirect,X	x	x	x	2	6 <sup>1,2</sup>
02	COP	Stack/Interrupt			x	2**	7 <sup>9</sup>
03	ORA	Stack Relative			x	2	4 <sup>1</sup>
04	TSB	Direct Page		x	x	2	5 <sup>2,5</sup>
05	ORA	Direct Page	x	x	x	2	3 <sup>1,2</sup>
06	ASL	Direct Page	x	x	x	2	5 <sup>2,5</sup>
07	ORA	DP Indirect Long			x	2	6 <sup>1,2</sup>
08	PHP	Stack (Push)	x	x	x	1	3
09	ORA	Immediate	x	x	x	2*	2 <sup>1</sup>
0A	ASL	Accumulator	x	x	x	1	2
0B	PHD	Stack (Push)			x	1	4
0C	TSB	Absolute		x	x	3	6 <sup>5</sup>
0D	ORA	Absolute	x	x	x	3	4 <sup>1</sup>
0E	ASL	Absolute	x	x	x	3	6 <sup>5</sup>
0F	ORA	Absolute Long			x	4	5 <sup>1</sup>
10	BPL	Program Counter Relative	x	x	x	2	2 <sup>7,8</sup>
11	ORA	DP Indirect Indexed,Y	x	x	x	2	5 <sup>1,2,3</sup>
12	ORA	DP Indirect		x	x	2	5 <sup>1,2</sup>
13	ORA	SR Indirect Indexed,Y			x	2	7 <sup>1</sup>
14	TRB	Direct Page		x	x	2	5 <sup>2,5</sup>
15	ORA	DP Indexed,X	x	x	x	2	4 <sup>1,2</sup>
16	ASL	DP Indexed,X	x	x	x	2	6 <sup>2,5</sup>
17	ORA	DP Indirect Long Indexed,Y			x	2	6 <sup>1,2</sup>
18	CLC	Implied	x	x	x	1	2
19	ORA	Absolute Indexed,Y	x	x	x	3	4 <sup>1,3</sup>
1A	INC	Accumulator		x	x	1	2
1B	TCS	Implied			x	1	2
1C	TRB	Absolute		x	x	3	6 <sup>5</sup>
1D	ORA	Absolute Indexed,X	x	x	x	3	4 <sup>1,3</sup>
1E	ASL	Absolute Indexed,X	x	x	x	3	7 <sup>5,6</sup>
1F	ORA	Absolute Long Indexed,X			x	4	5 <sup>1</sup>
20	JSR	Absolute	x	x	x	3	6
21	AND	DP Indexed Indirect,X	x	x	x	2	6 <sup>1,2</sup>

Opcode			Available on:			# of	# of
Hex	Mnemonic	Addressing Mode	6502	65C02	65802/816	Bytes	Cycles
22	JSR	Absolute Long			x	4	8
23	AND	Stack Relative			x	2	4 <sup>1</sup>
24	BIT	Direct Page	x	x	x	2	3 <sup>1,2</sup>
25	AND	Direct Page	x	x	x	2	3 <sup>1,2</sup>
26	ROL	Direct Page	x	x	x	2	5 <sup>2,5</sup>
27	AND	DP Indirect Long			x	2	6 <sup>1,2</sup>
28	PLP	Stack (Pull)	x	x	x	1	4
29	AND	Immediate	x	x	x	2*	2 <sup>1</sup>
2A	ROL	Accumulator	x	x	x	1	2
2B	PLD	Stack (Pull)			x	1	5
2C	BIT	Absolute	x	x	x	3	4 <sup>1</sup>
2D	AND	Absolute	x	x	x	3	4 <sup>1</sup>
2E	ROL	Absolute	x	x	x	3	6 <sup>5</sup>
2F	AND	Absolute Long			x	4	5 <sup>1</sup>
30	BMI	Program Counter Relative	x	x	x	2	2 <sup>7,8</sup>
31	AND	DP Indirect Indexed,Y	x	x	x	2	5 <sup>1,2,3</sup>
32	AND	DP Indirect		x	x	2	5 <sup>1,2</sup>
33	AND	SR Indirect Indexed,Y			x	2	7 <sup>1</sup>
34	BIT	DP Indexed,X		x	x	2	4 <sup>1,2</sup>
35	AND	DP Indexed,X	x	x	x	2	4 <sup>1,2</sup>
36	ROL	DP Indexed,X	x	x	x	2	6 <sup>2,5</sup>
37	AND	DP Indirect Long Indexed,Y			x	2	6 <sup>1,2</sup>
38	SEC	Implied	x	x	x	1	2
39	AND	Absolute Indexed,Y	x	x	x	3	4 <sup>1,3</sup>
3A	DEC	Accumulator		x	x	1	2
3B	TSC	Implied			x	1	2
3C	BIT	Absolute Indexed,X		x	x	3	4 <sup>1,3</sup>
3D	AND	Absolute Indexed,X	x	x	x	3	4 <sup>1,3</sup>
3E	ROL	Absolute Indexed,X	x	x	x	3	7 <sup>5,6</sup>
3F	AND	Absolute Long Indexed,X			x	4	5 <sup>1</sup>
40	RTI	Stack/RTI	x	x	x	1	6 <sup>9</sup>
41	EOR	DP Indexed Indirect,X	x	x	x	2	6 <sup>1,2</sup>
42	WDM				x	2 <sup>16</sup>	16
43	EOR	Stack Relative			x	2	4 <sup>1</sup>
44	MVP	Block Move			x	3	13
45	EOR	Direct Page	x	x	x	2	3 <sup>1,2</sup>
46	LSR	Direct Page	x	x	x	2	5 <sup>2,5</sup>
47	EOR	DP Indirect Long			x	2	6 <sup>1,2</sup>
48	PHA	Stack (Push)	x	x	x	1	3 <sup>1</sup>
49	EOR	Immediate	x	x	x	2*	2 <sup>1</sup>
4A	LSR	Accumulator	x	x	x	1	2

Opcode			Available on:			# of	# of
Hex	Mnemonic	Addressing Mode	6502	65C02	65802/816	Bytes	Cycles
4B	PHK	Stack (Push)			x	1	3
4C	JMP	Absolute	x	x	x	3	3
4D	EOR	Absolute	x	x	x	3	4 <sup>1</sup>
4E	LSR	Absolute	x	x	x	3	6 <sup>5</sup>
4F	EOR	Absolute Long			x	4	5 <sup>1</sup>
50	BVC	Program Counter Relative	x	x	x	2	2 <sup>7,8</sup>
51	EOR	DP Indirect Indexed, Y	x	x	x	2	5 <sup>1,2,3</sup>
52	EOR	DP Indirect		x	x	2	5 <sup>1,2</sup>
53	EOR	SR Indirect Indexed, Y			x	2	7 <sup>1</sup>
54	MVN	Block Move			x	3	13
55	EOR	DP Indexed, X	x	x	x	2	4 <sup>1,2</sup>
56	LSR	DP Indexed, X	x	x	x	2	6 <sup>2,5</sup>
57	EOR	DP Indirect Long Indexed, Y			x	2	6 <sup>1,2</sup>
58	CLI	Implied	x	x	x	1	2
59	EOR	Absolute Indexed, Y	x	x	x	3	4 <sup>1,3</sup>
5A	PHY	Stack (Push)		x	x	1	3 <sup>10</sup>
5B	TCD	Implied			x	1	2
5C	JMP	Absolute Long			x	4	4
5D	EOR	Absolute Indexed, X	x	x	x	3	4 <sup>1,3</sup>
5E	LSR	Absolute Indexed, X	x	x	x	3	7 <sup>5,6</sup>
5F	EOR	Absolute Long Indexed, X			x	4	5 <sup>1</sup>
60	RTS	Stack (RTS)	x	x	x	1	6
61	ADC	DP Indexed Indirect, X	x	x	x	2	6 <sup>1,2,4</sup>
62	PER	Stack (PC Relative Long)			x	3	6
63	ADC	Stack Relative			x	2	4 <sup>1,4</sup>
64	STZ	Direct Page		x	x	2	3 <sup>1,2</sup>
65	ADC	Direct Page	x	x	x	2	3 <sup>1,2,4</sup>
66	ROR	Direct Page	x	x	x	2	5 <sup>2,5</sup>
67	ADC	DP Indirect Long			x	2	6 <sup>1,2,4</sup>
68	PLA	Stack (Pull)	x	x	x	1	4 <sup>1</sup>
69	ADC	Immediate	x	x	x	2*	2 <sup>1,4</sup>
6A	ROR	Accumulator	x	x	x	1	2
6B	RTL	Stack (RTL)			x	1	6
6C	JMP	Absolute Indirect	x	x	x	3	5 <sup>11,12</sup>
6D	ADC	Absolute	x	x	x	3	4 <sup>1,4</sup>
6E	ROR	Absolute	x	x	x	3	6 <sup>5</sup>
6F	ADC	Absolute Long			x	4	5 <sup>1,4</sup>
70	BVS	Program Counter Relative	x	x	x	2	2 <sup>7,8</sup>
71	ADC	DP Indirect Indexed, Y	x	x	x	2	5 <sup>1,2,3,4</sup>
72	ADC	DP Indirect		x	x	2	5 <sup>1,2,4</sup>

Opcode			Available on:			# of	# of
Hex	Mnemonic	Addressing Mode	6502	65C02	65802/816	Bytes	Cycles
73	ADC	SR Indirect Indexed, Y			x	2	7 <sup>1,4</sup>
74	STZ	Direct Page Indexed, X		x	x	2	4 <sup>1,2</sup>
75	ADC	DP Indexed, X	x	x	x	2	4 <sup>1,2,4</sup>
76	ROR	DP Indexed, X	x	x	x	2	6 <sup>2,5</sup>
77	ADC	DP Indirect Long Indexed, Y			x	2	6 <sup>1,2,4</sup>
78	SEI	Implied	x	x	x	1	2
79	ADC	Absolute Indexed, Y	x	x	x	3	4 <sup>1,3,4</sup>
7A	PLY	Stack/Pull		x	x	1	4 <sup>10</sup>
7B	TDC	Implied			x	1	2
7C	JMP	Absolute Indexed Indirect		x	x	3	6
7D	ADC	Absolute Indexed, X	x	x	x	3	4 <sup>1,3,4</sup>
7E	ROR	Absolute Indexed, X	x	x	x	3	7 <sup>5,6</sup>
7F	ADC	Absolute Long Indexed, X			x	4	5 <sup>1,4</sup>
80	BRA	Program Counter Relative		x	x	2	3 <sup>8</sup>
81	STA	DP Indexed Indirect, X	x	x	x	2	6 <sup>1,2</sup>
82	BRL	Program Counter Relative Long			x	3	4
83	STA	Stack Relative			x	2	4 <sup>1</sup>
84	STY	Direct Page	x	x	x	2	3 <sup>2,10</sup>
85	STA	Direct Page	x	x	x	2	3 <sup>1,2</sup>
86	STX	Direct Page	x	x	x	2	3 <sup>2,10</sup>
87	STA	DP Indirect Long			x	2	6 <sup>1,2</sup>
88	DEY	Implied	x	x	x	1	2
89	BIT	Immediate		x	x	2*	2 <sup>1</sup>
8A	TXA	Implied	x	x	x	1	2
8B	PHB	Stack (Push)			x	1	3
8C	STY	Absolute	x	x	x	3	4 <sup>10</sup>
8D	STA	Absolute	x	x	x	3	4 <sup>1</sup>
8E	STX	Absolute	x	x	x	3	4 <sup>10</sup>
8F	STA	Absolute Long			x	4	5 <sup>1</sup>
90	BCC	Program Counter Relative	x	x	x	2	2 <sup>7,8</sup>
91	STA	DP Indirect Indexed, Y	x	x	x	2	6 <sup>1,2</sup>
92	STA	DP Indirect		x	x	2	5 <sup>1,2</sup>
93	STA	SR Indirect Indexed, Y			x	2	7 <sup>1</sup>
94	STY	Direct Page Indexed, X	x	x	x	2	4 <sup>2,10</sup>
95	STA	DP Indexed, X	x	x	x	2	4 <sup>1,2</sup>
96	STX	Direct Page Indexed, Y	x	x	x	2	4 <sup>2,10</sup>
97	STA	DP Indirect Long Indexed, Y			x	2	6 <sup>1,2</sup>
98	TYA	Implied	x	x	x	1	2
99	STA	Absolute Indexed, Y	x	x	x	3	5 <sup>1</sup>
9A	TXS	Implied	x	x	x	1	2
9B	TXY	Implied			x	1	2



Opcode			Available on:			# of	# of
Hex	Mnemonic	Addressing Mode	6502	65C02	65802/816	Bytes	Cycles
9C	STZ	Absolute		x	x	3	4 <sup>1</sup>
9D	STA	Absolute Indexed,X	x	x	x	3	5 <sup>1</sup>
9E	STZ	Absolute Indexed,X		x	x	3	5 <sup>1</sup>
9F	STA	Absolute Long Indexed,X			x	4	5 <sup>1</sup>
A0	LDY	Immediate	x	x	x	2 +	2 <sup>10</sup>
A1	LDA	DP Indexed Indirect,X	x	x	x	2	6 <sup>1,2</sup>
A2	LDX	Immediate	x	x	x	2 +	2 <sup>10</sup>
A3	LDA	Stack Relative			x	2	4 <sup>1</sup>
A4	LDY	Direct Page	x	x	x	2	3 <sup>2,10</sup>
A5	LDA	Direct Page	x	x	x	2	3 <sup>1,2</sup>
A6	LDX	Direct Page	x	x	x	2	3 <sup>2,10</sup>
A7	LDA	DP Indirect Long			x	2	6 <sup>1,2</sup>
A8	TAY	Implied	x	x	x	1	2
A9	LDA	Immediate	x	x	x	2*	2 <sup>1</sup>
AA	TAX	Implied	x	x	x	1	2
AB	PLB	Stack (Pull)			x	1	4
AC	LDY	Absolute	x	x	x	3	4 <sup>10</sup>
AD	LDA	Absolute	x	x	x	3	4 <sup>1</sup>
AE	LDX	Absolute	x	x	x	3	4 <sup>10</sup>
AF	LDA	Absolute Long			x	4	5 <sup>1</sup>
B0	BCS	Program Counter Relative	x	x	x	2	2 <sup>7,8</sup>
B1	LDA	DP Indirect Indexed,Y	x	x	x	2	5 <sup>1,2,3</sup>
B2	LDA	DP Indirect		x	x	2	5 <sup>1,2</sup>
B3	LDA	SR Indirect Indexed,Y			x	2	7 <sup>1</sup>
B4	LDY	DP Indexed,X	x	x	x	2	4 <sup>2,10</sup>
B5	LDA	DP Indexed,X	x	x	x	2	4 <sup>1,2</sup>
B6	LDX	DP Indexed,Y	x	x	x	2	4 <sup>2,10</sup>
B7	LDA	DP Indirect Long Indexed,Y			x	2	6 <sup>1,2</sup>
B8	CLV	Implied	x	x	x	1	2
B9	LDA	Absolute Indexed,Y	x	x	x	3	4 <sup>1,3</sup>
BA	TSX	Implied	x	x	x	1	2
BB	TYX	Implied			x	1	2
BC	LDY	Absolute Indexed,X	x	x	x	3	4 <sup>3,10</sup>
BD	LDA	Absolute Indexed,X	x	x	x	3	4 <sup>1,3</sup>
BE	LDX	Absolute Indexed,Y	x	x	x	3	4 <sup>3,10</sup>
BF	LDA	Absolute Long Indexed,X			x	4	5 <sup>1</sup>
C0	CPY	Immediate	x	x	x	2 +	2 <sup>10</sup>
C1	CMP	DP Indexed Indirect,X	x	x	x	2	6 <sup>1,2</sup>
C2	REP	Immediate			x	2	3
C3	CMP	Stack Relative			x	2	4 <sup>1</sup>

Opcode			Available on:			# of	# of
Hex	Mnemonic	Addressing Mode	6502	65C02	65802/816	Bytes	Cycles
C4	CPY	Direct Page	x	x	x	2	3 <sup>2,10</sup>
C5	CMP	Direct Page	x	x	x	2	3 <sup>1,2</sup>
C6	DEC	Direct Page	x	x	x	2	5 <sup>2,5</sup>
C7	CMP	DP Indirect Long			x	2	6 <sup>1,2</sup>
C8	INY	Implied	x	x	x	1	2
C9	CMP	Immediate	x	x	x	2*	2 <sup>1</sup>
CA	DEX	Implied	x	x	x	1	2
CB	WAI	Implied			x	1	3 <sup>15</sup>
CC	CPY	Absolute	x	x	x	3	4 <sup>10</sup>
CD	CMP	Absolute	x	x	x	3	4 <sup>1</sup>
CE	DEC	Absolute	x	x	x	3	6 <sup>5</sup>
CF	CMP	Absolute Long			x	4	5 <sup>1</sup>
D0	BNE	Program Counter Relative	x	x	x	2	2 <sup>7,8</sup>
D1	CMP	DP Indirect Indexed,Y	x	x	x	2	5 <sup>1,2,3</sup>
D2	CMP	DP Indirect		x	x	2	5 <sup>1,2</sup>
D3	CMP	SR Indirect Indexed,Y			x	2	7 <sup>1</sup>
D4	PEI	Stack (Direct Page Indirect)			x	2	6 <sup>2</sup>
D5	CMP	DP Indexed,X	x	x	x	2	4 <sup>1,2</sup>
D6	DEC	DP Indexed,X	x	x	x	2	6 <sup>2,5</sup>
D7	CMP	DP Indirect Long Indexed,Y			x	2	6 <sup>1,2</sup>
D8	CLD	Implied	x	x	x	1	2
D9	CMP	Absolute Indexed,Y	x	x	x	3	4 <sup>1,3</sup>
DA	PHX	Stack (Push)		x	x	1	3 <sup>10</sup>
DB	STP	Implied			x	1	3 <sup>14</sup>
DC	JMP	Absolute Indirect Long			x	3	6
DD	CMP	Absolute Indexed,X	x	x	x	3	4 <sup>1,3</sup>
DE	DEC	Absolute Indexed,X	x	x	x	3	7 <sup>5,6</sup>
DF	CMP	Absolute Long Indexed,X			x	4	5 <sup>1</sup>
E0	CPX	Immediate	x	x	x	2 +	2 <sup>10</sup>
E1	SBC	DP Indexed Indirect,X	x	x	x	2	6 <sup>1,2,4</sup>
E2	SEP	Immediate			x	2	3
E3	SBC	Stack Relative			x	2	4 <sup>1,4</sup>
E4	CPX	Direct Page	x	x	x	2	3 <sup>2,10</sup>
E5	SBC	Direct Page	x	x	x	2	3 <sup>1,2,4</sup>
E6	INC	Direct Page	x	x	x	2	5 <sup>2,5</sup>
E7	SBC	DP Indirect Long			x	2	6 <sup>1,2,4</sup>
E8	INX	Implied	x	x	x	1	2
E9	SBC	Immediate	x	x	x	2*	2 <sup>1,4</sup>
EA	NOP	Implied	x	x	x	1	2
EB	XBA	Implied			x	1	3
EC	CPX	Absolute	x	x	x	3	4 <sup>10</sup>

Opcode			Available on:			# of	# of
Hex	Mnemonic	Addressing Mode	6502	65C02	65802/816	Bytes	Cycles
ED	SBC	Absolute	x	x	x	3	4 <sup>1,4</sup>
EE	INC	Absolute	x	x	x	3	6 <sup>5</sup>
EF	SBC	Absolute Long			x	4	5 <sup>1,4</sup>
F0	BEQ	Program Counter Relative	x	x	x	2	2 <sup>7,8</sup>
F1	SBC	DP Indirect Indexed,Y	x	x	x	2	5 <sup>1,2,3,4</sup>
F2	SBC	DP Indirect		x	x	2	5 <sup>1,2,4</sup>
F3	SBC	SR Indirect Indexed,Y			x	2	7 <sup>1,4</sup>
F4	PEA	Stack (Absolute)			x	3	5
F5	SBC	DP Indexed,X	x	x	x	2	4 <sup>1,2,4</sup>
F6	INC	DP Indexed,X	x	x	x	2	6 <sup>2,5</sup>
F7	SBC	DP Indirect Long Indexed,Y			x	2	6 <sup>1,2,4</sup>
F8	SED	Implied	x	x	x	1	2
F9	SBC	Absolute Indexed,Y	x	x	x	3	4 <sup>1,3,4</sup>
FA	PLX	Stack/Pull		x	x	1	4 <sup>10</sup>
FB	XCE	Implied			x	1	2
FC	JSR	Absolute Indexed Indirect			x	3	8
FD	SBC	Absolute Indexed,X	x	x	x	3	4 <sup>1,3,4</sup>
FE	INC	Absolute Indexed,X	x	x	x	3	7 <sup>5,6</sup>
FF	SBC	Absolute Long Indexed,X			x	4	5 <sup>1,4</sup>

\* Add 1 byte if m = 0 (16-bit memory/accumulator)

\*\* opcode is 1 byte, but program counter value pushed onto stack is incremented by 2 allowing for optional signature byte

+ Add 1 byte if x = 0 (16-bit index registers)

1 Add 1 cycle if m = 0 (16-bit memory/accumulafor)

2 Add 1 cycle if low byte of Direct Page register is other than zero (DL< >0)

3 Add 1 cycle if adding index crosses a page boundary

4 Add 1 cycle if 65C02 and d = 1 (decimal mode, 65C02)

5 Add 2 cycles if m = 0 (16-bit memory/accumulator)

6 Subtract 1 cycle if 65C02 and no page boundary crossed

7 Add 1 cycle if branch is taken

8 Add 1 more cycle if branch taken crosses page boundary on 6502, 65C02, or 65816/65802's 6502 emulation mode (e = 1)

9 Add 1 cycle for 65802/65816 native mode (e = 0)

10 Add 1 cycle if x = 0 (16-bit index registers)

11 Add 1 cycle if 65C02

12 6502: If low byte of operand is \$FF ( i.e., operand is SxxFF): yields incorrect result

13 7 cycles per byte moved

14 Uses 3 cycles to shut the processor down; additional cycles are required by reset to restart it

15 Uses 3 cycles to shut the processor down; additional cycles are required by interrupt to restart it

10 Byte and cycle counts subject to change in future processors which expand WDM into 2-byte opcode portions of instructions of varying lengths