Mnemonic	Desctiption	Example	Parameters	Flags affected
ADC r	Add register r and the carry flag to the Accumulator A.	ADC B	'r': (HL) (IX+#) (IY+#) A B C D E H L IXH IXL IYH IYL	S Z H V N C
ADC A,#	Add 8 bit number # and the carry to A.	ADC 128	'#': 0-255 ($00-$FF)	S Z H V N C
ADC HL,rr	Add 16 bit register rr and the carry to HL.	ADC HL,BC	'rr': BC DE HL SP	S Z H V N C
ADD rr2,rr1	Add 16 bit register rr1 to 16 bit register rr2.	ADD HL,BC	'rr1': HL IX IY 'rr2': BC DE SP *HL IX IY*	- - H - N C
ADD r	Adds 8 bit register r to A.	ADD B	'r': (HL) (IX+#) (IY+#) A B C D E H L IXH IXL IYH IYL	S Z H V N C
ADD #	Adds 8 bit value # to A.	ADD B	'#': 0-255 ($00-$FF)	S Z H V N C
AND r	Logical AND of bits in register r with Accumulator A.	AND B	'r': (HL) (IX+#) (IY+#) A B C D E H L IXH IXL IYH IYL	S Z H V N C
AND #	Logical AND of bits in 8 bit value # with Accumulator A.	AND $64	'#': 0-255 ($00-$FF)	S Z H V N C
BIT b,r	Test bit b from 8 bit register r and set the Z flag to that bit.	BIT 7,B	'b': 0-7 (%76543210) 'r': (HL) (IX+#) (IY+#) A B C D E H L	s Z H v N -
CALL addr	Call Subroutine at address addr	CALL $1000	'addr': 0-65535 ($0000-$FFFF)	- - - - - -
CALL c,addr	Call Subroutine at address addr only IF condition c is true.	CALL Z,$1000	'addr': 0-65535 ($0000-$FFFF) 'c': c m nc nz p po pe z	- - - - - -
CCF	Complement the Carry Flag. C flag will inverted	CCF		- - H - N C
CP r	Compare the Accumulator to register r.	CP B	'r': (HL) (IX+#) (IY+#) A B C D E H L	S Z H V N C
CP #	Compare the Accumulator to 8 bit immediate value #.	CP 32	'#':0-255 ($00-$FF)	S Z H V N C
CPD	Compare A to the byte at address HL and decrease HL and BC.	CPD		S Z H V N -
CPDR	Compare A to the byte at address HL and Decrease and Repeat	CPDR		S Z H V N -
CPI	Compare A to the byte at address HL and increase HL but decrease BC (Bytecount).	CPI		S Z H V N -
CPIR	Compare A to the byte at addr HL and inc HL dec BC (Bytecount) and Rep until match or BC=0.	CPIR		S Z H V N -
CPL	Invert all bits of A (this is known as 'One's Complement').	CPL		- - H - N -
DAA	Decimal Adjust Accumulator (Binary Coded Decimal)	DAA		S Z H V - C
DEC r	Decrease value in 8 bit register r by one.	DEC B	'r': (HL) (IX+#) (IY+#) A B C D E H L IXH IXL IYH IYL	S Z H V N -
DEC rr	Decrease value in 16 bit register rr by one.	DEC HL	Valid registers for 'rr': BC DE HL IX IY SP	- - - - - -
DI	Disable Maskable Interrupts	DI		- - - - - -
DJNZ ofst	Decrease B and Jump if NonZero to address offset #.	DJNZ label	'ofst': -128 to +127	- - - - - -
EI	Enable Maskable Interrupts.	EI		- - - - - -
EX (SP),HL	Exchange HL with the top item of the stack	EX (SP),HL		- - - - - -
EX AF,AF'	Exchange the Accumulator and Flags with the shadow Accumulator and Flags.	EX AF,AF'		S Z H V N C
EX DE,HL	Exchange HL and DE	EX DE,HL		- - - - - -
EXX	Exchange the registers BC, DE and HL with the shadow registers	EXX		- - - - - -
HALT	Stop the CPU until an interrupt occurs.	HALT		- - - - - -
IM0	Enable Interrupt mode 0.	IM0		- - - - - -
IM1	Enable Interrupt mode 1.	IM1		- - - - - -
IM2	Enable Interrupt mode 2.	IM2		- - - - - -
IN A,(#)	Read in an 8 bit byte A from 8 bit port #.	IN A,($10)	'#': 0-255 ($00-$FF)	S Z H V N -
IN r,(C)	Read in an 8 bit byte into register r from port (C)	IN A,(C)	'r': A B C D E H L	S Z H V N -
INC r	Increase value in 8 bit register r by one.	INC B	'r': (HL) (IX+#) (IY+#) A B C D E H L IXH IXL IYH IYL	S Z H V N -
INC rr	Increase value in 16 bit register r by one.	INC HL	'rr': BC DE HL IX IY SP	- - - - - -
IND	Read a byte IN from port (C) and save to address in HL, then Decrease HL and B.	IND		s Z h v N -
INDR	Read a byte IN from port (C) and save to address in HL. then Decrease HL and B, rep until B=0.	INDR		s Z h v N -
INI	Read a byte IN from port (C) and save to address in HL, then increase HL and decrease B.	INI		s Z h v N -
INIR	Read a byte IN from port (C) and save to the address in HL, inc HL and dec B, rep until B=0.	INIR		s Z h v N -
JP (HL)	Jump to the address in register HL.	JP (HL)		- - - - - -
JP addr	Jump to the 16 bit address addr.	JP $4000	'addr': 0-65535 ($0000-$FFFF)	- - - - - -
JP c,addr	Jump to the 16 bit address addr only IF condition c is true in the flags register.	JP Z,$4000	'addr': 0-65535 ($0000-$FFFF) 'c': c m nc nz p po pe z	- - - - - -
JR ofst	Jump to the 8 bit offset #.	JR TestLabel	'#': -128 to +127	- - - - - -
JR c,ofst	Jump to the 8 bit offset ofst IF condition c is true.	JR Z,TestLabel	'ofst': -128 to +127	- - - - - -
LD (rr),A	Load the 8 bit value in the Accumulator into the address in register rr.	LD (DE),A	'rr': BC DE HL IX+# IY SP	- - - - - -
LD (HL),B	Load the 8 bit value in register r into the address in register rr.	LD (HL),B	'r': A B C D E H L 'rr': HL IX+# IY+#	- - - - - -
LD (addr),A	Load the 8 bit value in the Accumulator into memory address addr.	LD ($C000),A	'addr': 0-65535 ($0000-$FFFF)	- - - - - -
LD (addr),rr	Load the 16 bit value in register pair rr into memory address addr.	LD ($C000),BC	'addr': 0-65535 ($0000-$FFFF) 'rr': BC DE HL IX IY SP	- - - - - -
LD A,(rr)	Load the 8 bit value from the address in register rr into the Accumulator.	LD A,(DE)	'rr': BC DE HL IX+# IY SP	- - - - - -
LD A,(addr)	Load the 8 bit value from memory address addr into the Accumulator.	LD A,($C000)	'##': 0-65535 ($0000-$FFFF)	- - - - - -
LD r,#	Load the 8 bit register r with value #.	LD B,32	'r': A B C D E H L IXH IXL IYH IYL '#': 0-255 ($00-$FF)	- - - - - -
LD A,I	Load the 8 bit value from the I register to the Accumulator.	LD A,I		S Z H V N -
LD A,R	Load the 8 bit value from the R register to the Accumulator.	LD A,R		S Z H V N -
LD rr,(addr)	Load the 16 bit register pair rr from memory address addr.	LD BC,($C000)	'rr': BC DE HL IX IY SP 'addr': 0-65535 ($0000-$FFFF)	- - - - - -
LD rr,####	Load the 16 bit register pair rr with immediate value ####	LD BC,$C000	'rr': BC DE HL IX IY SP 'addr': 0-65535 ($0000-$FFFF)	- - - - - -
LD I,A	Load the 8 bit value from the Accumulator into the I register.	LD I,A		- - - - - -
LD R,A	Load the R register with the 8 bit value in the Accumulator.	LD R,A		- - - - - -
LD SP,HL	Load the 16 bit Stack Pointer register SP with the value in HL.	LD SP,HL		- - - - - -
LD r1,r2	Load the 8 bit register r1 from register r2.	LD H,B	'r1' and 'r2': A B C D E H L IXH IXL IYH IYL	- - - - - -
LD r,(rr)	Load the 8 bit register r from the address in register rr.	LD B,(HL)	'r': A B C D E H L 'rr': HL IX+# IY+#	- - - - - -
LDD	Load and Decrement. Copies bytes down from HL to DE with BC as a byte count.	LDD		- - H V N -
LDDR	Load, Decrement and Repeat. Copies bytes down from HL to DE with BC as a Byte count	LDDR		- - H V N -
LDI	Load and Increment. Copies bytes upwards from HL to DE with BC as a byte count	LDI		- - H V N -
LDIR	Load, Decrement and Repeat. Copies bytes upwards from HL to DE with BC as byte count	LDIR		- - H V N -
NEG	Negate the 8 bit value in the accumulator (Two's Complement of the number).	NEG		S Z H V N C
NOP	No Operation. This command has no effect on any registers or memory.	NOP		- - - - - -
OR r	Logical OR of bits in register r with Accumulator A.	OR B	'r': (HL) (IX+#) (IY+#) A B C D E H L IXH IXL IYH IYL	S Z H V N C
OR #	Logical OR of bits in 8 bit value # with Accumulator A.	OR $64	'#': 0-255 ($00-$FF)	S Z H V N C
OTDR	Out Decrement Repeat. Transfers B bytes from HL to port (C) moving downwards.	OTDR		s Z h v N -
OTIR	Out Increment Repeat. This command transfers B bytes from HL to port (C) moving upwards.	OTIR		s Z h v N -
OUT (#),A	Output an 8 bit byte from A to 8 bit port #.	OUT ($10),A	'#': 0-255 ($00-$FF)	- - - - - -
OUT (C),r	On a system with 8 bit ports, this will output an 8 bit byte from register r to port (C) .	OUT (C),r	'r': A B C D E H L	- - - - - -
OUT (C),0	On a system with 8 bit ports, this will output an 8 bit byte zero to port (C).	OUT (C),0		- - - - - -
OUTD	Out and Decrement. This command transfers a byte from HL to port (C) moving downwards.	OUTD		s Z h v N -
OUTI	Out and Increment. This command transfers a byte from HL to port (C) moving upwards.	OUTI		s Z h v N -
POP rr	Pop a pair of bytes off the stack into 16 bit register rr.	POP AF	'rr': AF BC DE HL IX IY	all if AF / none
PUSH rr	Push a pair of bytes from 16 bit register rr onto the top of the stack.	PUSH AF	'rr': AF BC DE HL IX IY	- - - - - -
RES b,r	Reset bit b from 8 bit register r to 0.	RES 7,B	'b': 0-7 (%76543210) 'r': (HL) (IX+#) (IY+#) A B C D E H L	- - - - - -
RET	Return from a subroutine.	RET		- - - - - -
RET c	Return from a subroutine only if condition c is true.	RET Z	'c': c m nc nz p po pe z	- - - - - -
RETI	Return from an interrupt.	RETI		- - - - - -
RETN	Return from a non maskable interrupt (NMI).	RETN		- - - - - -
RL r	Rotate bits in register r Left with Carry.	RL B	'r': (HL) (IX+#) (IY+#) A B C D E H L	S Z H P N C
RLC r	Rotate bits in register r Left and Copy the top bit to the Carry.	RLC B	'r': (HL) (IX+#) (IY+#) A B C D E H L	S Z H P N C
RLD	Rotate Left for binary coded Decimal.	RLD		S Z H V N -
RR r	Rotate bits in register r Right with carry.	RR B	'r': (HL) (IX+#) (IY+#) A B C D E H L	S Z H P N C
RRC r	Rotate bits in register r Right and Copy the bottom bit to the Carry.	RLC B	'r': (HL) (IX+#) (IY+#) A B C D E H L	S Z H P N C
RRD	Rotate Right for binary coded Decimal.	RRD		S Z H V N -
RST #	ReSeT function. RST is a single byte call to $00xx address.	RST $38		- - - - - -
SBC r	Subtract register r and the carry flag from the Accumulator A.	SBC B	'r': (HL) (IX+#) (IY+#) A B C D E H L IXH IXL IYH IYL	S Z H V N C
SBC A,#	Subtract 8 bit number # and the carry from A.	SBC 128	'#': 0-255 ($00-$FF)	S Z H V N C
SBC HL,rr	Subtract 16 bit register rr and the carry from HL.	SBC HL,BC	'rr': BC DE HL SP	S Z H V N C
SCF	Set the carry flag to 1.	SCF		- - H - N C
SET b,r	Set bit b from 8 bit register r to 1.	SET 7,B	'b': 0-7 (%76543210) 'r': (HL) (IX+#) (IY+#) A B C D E H L	- - - - - -
SLA r	Shift the bits register r Left for Arithmetic.	SLA A	'r': (HL) (IX+#) (IY+#) A B C D E H L	S Z H P N C
SLL r	Shift the bits in register r Left Logically (for unsigned numbers).	SLL A	'r': (HL) (IX+#) (IY+#) A B C D E H L	S Z H P N C
SRA r	Shift the bits in register r Right for Arithmetic. '	SRA A	'r': (HL) (IX+#) (IY+#) A B C D E H L	S Z H P N C
SRL r	Shift the bits in register r Right Logically.	SRL A	'r': (HL) (IX+#) (IY+#) A B C D E H L	S Z H P N C
SUB r	Subtract 8 bit register r from A.	SUB B	'r': (HL) (IX+#) (IY+#) A B C D E H L IXH IXL IYH IYL	S Z H V N C
SUB #	Subtract 8 bit value # from A.	SUB 32	'#': 0-255 ($00-$FF)	S Z H V N C
XOR r	Logical XOR (eXclusive OR) of bits in register r with Accumulator A.	XOR B	'r': (HL) (IX+#) (IY+#) A B C D E H L IXH IXL IYH IYL	S Z H V N C
XOR #	Logical XOR (eXclusive OR) of bits in immediate value # with Accumulator A.	XOR $64	'#': 0-255 ($00-$FF)	S Z H V N C

Instruction	Opcodes	B / T	Flags
ADC A,(HL)	8E	1 / 7	- z v c
ADC A,(IX+d)	DD 8E d	3 / 19	- z v c
ADC A,(IY+d)	FD 8E d	3 / 19	- z v c
ADC A,A	8F	1 / 4	- z v c
ADC A,B	88	1 / 4	- z v c
ADC A,C	89	1 / 4	- z v c
ADC A,D	8A	1 / 4	- z v c
ADC A,E	8B	1 / 4	- z v c
ADC A,H	8C	1 / 4	- z v c
ADC A,IXH	DD 8C	2 / 8	- z v c
ADC A,IYH	FD 8C	2 / 8	- z v c
ADC A,L	8D	1 / 4	- z v c
ADC A,IXL	DD 8D	2 / 8	- z v c
ADC A,IYL	FD 8D	2 / 8	- z v c
ADC A,n	CE n	2 / 7	- z v c
ADC HL,BC	ED 4A	2 / 15	- z v c
ADC HL,DE	ED 5A	2 / 15	- z v c
ADC HL,HL	ED 6A	2 / 15	- z v c
ADC HL,SP	ED 7A	2 / 15	- z v c
ADD A,(HL)	86	1 / 7	- z v c
ADD A,(IX+d)	DD 86 d	3 / 19	- z v c
ADD A,(IY+d)	FD 86 d	3 / 19	- z v c
ADD A,A	87	1 / 4	- z v c
ADD A,B	80	1 / 4	- z v c
ADD A,C	81	1 / 4	- z v c
ADD A,D	82	1 / 4	- z v c
ADD A,E	83	1 / 4	- z v c
ADD A,H	84	1 / 4	- z v c
ADD A,IXH	DD 84	2 / 8	- z v c
ADD A,IYH	FD 84	2 / 8	- z v c
ADD A,L	85	1 / 4	- z v c
ADD A,IXL	DD 85	2 / 8	- z v c
ADD A,IYL	FD 85	2 / 8	- z v c
ADD A,n	C6 n	2 / 7	- z v c
ADD HL,BC	09	1 / 11	- - - c
ADD HL,DE	19	1 / 11	- - - c
ADD HL,HL	29	1 / 11	- - - c
ADD HL,SP	39	1 / 11	- - - c
ADD IX,BC	DD 09	2 / 15	- - - c
ADD IX,DE	DD 19	2 / 15	- - - c
ADD IX,IX	DD 29	2 / 15	- - - c
ADD IX,SP	DD 39	2 / 15	- - - c
ADD IY,BC	FD 09	2 / 15	- - - c
ADD IY,DE	FD 19	2 / 15	- - - c
ADD IY,IY	FD 29	2 / 15	- - - c
ADD IY,SP	FD 39	2 / 15	- - - c
ADD SP,n	E8 n	1 / 16	n z v c
AND (HL)	A6	1 / 7	- z p c
AND (IX+d)	DD A6 d	3 / 19	- z p c
AND (IY+d)	FD A6 d	3 / 19	- z p c
AND A	A7	1 / 4	- z p c
AND B	A0	1 / 4	- z p c
AND C	A1	1 / 4	- z p c
AND D	A2	1 / 4	- z p c
AND E	A3	1 / 4	- z p c
AND H	A4	1 / 4	- z p c
AND IXH	DD A4	2 / 8	- z v c
AND IYH	FD A4	2 / 8	- z v c
AND L	A5	1 / 4	- z p c
AND IXL	DD A5	2 / 8	- z v c
AND IYL	FD A5	2 / 8	- z v c
AND n	E6 n	2 / 7	- z p c
BIT 0,(HL)	CB 46	2 / 12	? <>b ? -
BIT 0,(IX+d)	CB DD46 d	4 / 20	? <>b ? -
BIT 0,(IY+d)	CB FD46 d	4 / 20	? <>b ? -
BIT 0,A	CB 47	2 / 8	? <>b ? -
BIT 0,B	CB 40	2 / 8	? <>b ? -
BIT 0,C	CB 41	2 / 8	? <>b ? -
BIT 0,D	CB 42	2 / 8	? <>b ? -
BIT 0,E	CB 43	2 / 8	? <>b ? -
BIT 0,H	CB 44	2 / 8	? <>b ? -
BIT 0,L	CB 45	2 / 8	? <>b ? -
BIT 1,(HL)	CB 4E	2 / 12	? <>b ? -
BIT 1,(IX+d)	CB DD4E d	4 / 20	? <>b ? -
BIT 1,(IY+d)	CB FD4E d	4 / 20	? <>b ? -
BIT 1,A	CB 1F	2 / 8	? <>b ? -
BIT 1,B	CB 48	2 / 8	? <>b ? -
BIT 1,C	CB 49	2 / 8	? <>b ? -
BIT 1,D	CB 4A	2 / 8	? <>b ? -
BIT 1,E	CB 4B	2 / 8	? <>b ? -
BIT 1,H	CB 4C	2 / 8	? <>b ? -
BIT 1,L	CB 4D	2 / 8	? <>b ? -
BIT 2,(HL)	CB 56	2 / 12	? <>b ? -
BIT 2,(IY+d)	CB FD56 d	4 / 20	? <>b ? -
BIT 2,(LY+d)	CB DD56 d	4 / 20	? <>b ? -
BIT 2,A	CB 57	2 / 8	? <>b ? -
BIT 2,B	CB 50	2 / 8	? <>b ? -
BIT 2,C	CB 51	2 / 8	? <>b ? -
BIT 2,D	CB 52	2 / 8	? <>b ? -
BIT 2,E	CB 53	2 / 8	? <>b ? -
BIT 2,H	CB 54	2 / 8	? <>b ? -
BIT 2,L	CB 55	2 / 8	? <>b ? -
BIT 3,(HL)	CB 5E	2 / 12	? <>b ? -
BIT 3,(IX+d)	CB DD5E d	4 / 20	? <>b ? -
BIT 3,(IY+d)	CB FD5E d	4 / 20	? <>b ? -
BIT 3,A	CB 5F	2 / 8	? <>b ? -
BIT 3,B	CB 58	2 / 8	? <>b ? -
BIT 3,C	CB 59	2 / 8	? <>b ? -
BIT 3,D	CB 5A	2 / 8	? <>b ? -
BIT 3,E	CB 5B	2 / 8	? <>b ? -
BIT 3,H	CB 5C	2 / 8	? <>b ? -
BIT 3,L	CB 5D	2 / 8	? <>b ? -
BIT 4,(HL)	CB 66	2 / 12	? <>b ? -
BIT 4,(IY+d)	CB FD66 d	4 / 20	? <>b ? -
BIT 4,(LY+d)	CB DD66 d	4 / 20	? <>b ? -
BIT 4,A	CB 67	2 / 8	? <>b ? -
BIT 4,B	CB 60	2 / 8	? <>b ? -
BIT 4,C	CB 61	2 / 8	? <>b ? -
BIT 4,D	CB 62	2 / 8	? <>b ? -
BIT 4,E	CB 63	2 / 8	? <>b ? -
BIT 4,H	CB 64	2 / 8	? <>b ? -
BIT 4,L	CB 65	2 / 8	? <>b ? -
BIT 5,(HL)	CB 6E	2 / 12	? <>b ? -
BIT 5,(IX+d)	CB DD6E d	4 / 20	? <>b ? -
BIT 5,(IY+d)	CB FD6E d	4 / 20	? <>b ? -
BIT 5,A	CB 6F	2 / 8	? <>b ? -
BIT 5,B	CB 68	2 / 8	? <>b ? -
BIT 5,C	CB 69	2 / 8	? <>b ? -
BIT 5,D	CB 6A	2 / 8	? <>b ? -
BIT 5,E	CB 6B	2 / 8	? <>b ? -
BIT 5,H	CB 6C	2 / 8	? <>b ? -
BIT 5,L	CB 6D	2 / 8	? <>b ? -
BIT 6,(HL)	CB 76	2 / 12	? <>b ? -
BIT 6,(IX+d)	CB DD76 d	4 / 20	? <>b ? -
BIT 6,(IY+d)	CB FD76 d	4 / 20	? <>b ? -
BIT 6,A	CB 77	2 / 8	? <>b ? -
BIT 6,B	CB 70	2 / 8	? <>b ? -
BIT 6,C	CB 71	2 / 8	? <>b ? -
BIT 6,D	CB 72	2 / 8	? <>b ? -
BIT 6,E	CB 73	2 / 8	? <>b ? -
BIT 6,H	CB 74	2 / 8	? <>b ? -
BIT 6,L	CB 75	2 / 8	? <>b ? -
BIT 7,(HL)	CB 7E	2 / 12	? <>b ? -
BIT 7,(IX+d)	CB DD7E d	4 / 20	? <>b ? -
BIT 7,(IY+d)	CB FD7E d	4 / 20	? <>b ? -
BIT 7,A	CB 7F	2 / 8	? <>b ? -
BIT 7,B	CB 78	2 / 8	? <>b ? -
BIT 7,C	CB 79	2 / 8	? <>b ? -
BIT 7,D	CB 7A	2 / 8	? <>b ? -
BIT 7,E	CB 7B	2 / 8	? <>b ? -
BIT 7,H	CB 7C	2 / 8	? <>b ? -
BIT 7,L	CB 7D	2 / 8	? <>b ? -

Instruction	Opcodes	B / T	Flags
CALL addr	CD dr ad	3 / 17 20	- - - -
CALL c,addr	DC dr ad	3 / t17f10 12/20	- - - -
CALL m,addr	FC dr ad	3 / t17f10 12/20	- - - -
CALL nc,addr	D4 dr ad	3 / t17f10 12/20	- - - -
CALL nz,addr	C4 dr ad	3 / t17f10 12/20	- - - -
CALL p,addr	F4 dr ad	3 / t17f10 12/20	- - - -
CALL po,addr	E4 dr ad	3 / t17f10 12/20	- - - -
CALL pe,addr	EC dr ad	3 / t17f10 12/20	- - - -
CALL z,addr	CC dr ad	3 / t17f10 12/20	- - - -
CCF	3F	1 / 4	- - - x
CP (HL)	BE	1 / 7	- = v <
CP (IX+d)	DD BE d	3 / 19	- = v <
CP (IY+d)	FD BE d	3 / 19	- = v <
CP A	BF	1 / 4	- = v <
CP B	B8	1 / 4	- = v <
CP C	B9	1 / 4	- = v <
CP D	BA	1 / 4	- = v <
CP E	BB	1 / 4	- = v <
CP H	BC	1 / 4	- = v <
CP IXH	DD BC	2 / 8	- = v <
CP IYH	FD BC	2 / 8	- = v <
CP L	BD	1 / 4	- = v c
CP IXL	DD BD	2 / 8	- = v <
CP IYL	FD BD	2 / 8	- = v <
CP n	FE n	2 / 7	- = v <
CPD	ED A9	2 / 16	? - BC -
CPDR	ED B9	2 / =16#21	? - BC -
CPI	ED A1	2 / 16	? - BC -
CPIR	ED B2	2 / =16#21	? - BC -
CPL	2F	1 / 4	- - - -
DAA	27	1 / 4	- z p c
DEC (HL)	35	1 / 11	- z v -
DEC (IX+d)	DD 35d	3 / 23	- z v -
DEC (IY+d)	FD 35d	3 / 23	- z v -
DEC A	3D	1 / 4	- z v -
DEC B	5	1 / 4	- z v -
DEC BC	0B	1 / 6	- - - BUG
DEC C	0D	1 / 4	- z v -
DEC D	15	1 / 4	- z v -
DEC DE	1B	I / 6	- - - BUG
DEC E	1D	1 / 4	- z v -
DEC H	25	1 / 4	- z v -
DEC IXH	DD 25	2 / 8	- z v -
DEC IYH	FD 25	2 / 8	- z v -
DEC HL	2B	1 / 6	- - - BUG
DEC IX	DD 2B	2 / 10 12	- - - -
DEC IY	FD 2B	2 / 10 12	- - - -
DEC L	2D	1 / 4	- z v -
DEC IXL	DD 2D	2 / 8	- z v -
DEC IYL	FD 2D	2 / 8	- z v -
DEC SP	3B	1 / 6	- - - -
DI	F3	1 / 4	- - - -
DJNZ d	10 d	2 / t13f8	- - - -
EI	FB	1 / 4	- - - -
EX (SP),HL	E3	1 / 19	- - - -
EX (SP),IX	DD E3	2 / 23	- - - -
EX (SP),IY	FD E3	2 / 23	- - - -
EX AF,AF'	8	1 / 4	s' z' p' c'
EX DE,HL	EB	1 / 4	- - - -
EXX	D9	1 / 4	- - - -
HALT	76	1 / min 4	- - - BUG
IM 0	ED 46	2 / 8	- - - -
IM 1	ED 56	2 / 8	- - - -
IM 2	ED 5E	2 / 8	- - - -
IN A,(C)	ED 78	2 / 12 16	- z p -
IN A,(n)	DB n	2 / 11 12	- - - -
IN B,(C)	ED 40	2 / 12 16	- z p -
IN C,(C)	ED 48	2 / 12 16	- z p -
IN D,(C)	ED 50	2 / 12 16	- z p -
IN E,(C)	ED 58	2 / 12 16	- z p -
IN H,(C)	ED 60	2 / 12 16	- z p -
IN L,(C)	ED 68	2 / 12 16	- z p -
INC (HL)	34	1 / 11 12	- z v -
INC (IX+d)	DD 34 d	3 / 23 24	- z v -
INC (IY+d)	FD 34 d	3 / 23 24	- z v -
INC A	3C	1 / 4	- z v -
INC B	4	1 / 4	- z v -
INC BC	3	1 / 6 8	- - - BUG
INC C	0C	1 / 4	- z v -
INC D	14	1 / 4	- z v -
INC DE	13	1 / 6 8	- - - BUG
INC E	1C	1 / 4	- z v -
INC H	24	1 / 4	- z v -
INC IXH	DD 24	2 / 8	- z v -
INC IYH	FD 24	2 / 8	- z v -
INC HL	23	1 / 6 8	- - - BUG
INC IX	DD 23	2 / 10	- - - -
INC IY	FD 23	2 / 10	- - - -
INC L	2C	1 / 4	- z v -
INC IXL	DD 2C	2 / 8	- z v -
INC IYL	FD 2C	2 / 8	- z v -
INC SP	33	1 / 6	- - - -
IND	ED AA	2 / 16 25	? <>B ? -
INDR	ED BA	2 / z16nz21	? - ? -
INI	ED A2	2 / 16 25	? <>B ? -
INIR	ED B2	2 / z16nz21	? - ? -
JP (HL)	E9	1 / 4	- - - -
JP (IX)	DD E9	2 / 8	- - - -
JP (IY)	FD E9	2 / 8	- - - -
JP addr	C3 dr ad	3 / 10 12	- - - -
JP c,addr	DA dr ad	3 / 10 12	- - - -
JP m,addr	FA dr ad	3 / 10 12	- - - -
JP nc,addr	D2 dr ad	3 / 10 12	- - - -
JP nz,addr	C2 dr ad	3 / 10 12	- - - -
JP p,addr	F2 dr ad	3 / 10 12	- - - -
JP po,addr	E2 dr ad	3 / 10 12	- - - -
JP pe,addr	EA dr ad	3 / 10 12	- - - -
JP z,addr	CA dr ad	3 / 10 12	- - - -
JR c,d	38 d	2 / t12f7 8/12	- - - -
JR d	18 d	2 / 12	- - - -
JR nc,d	30 d	2 / t12f7 8/12	- - - -
JR nz,d	20 d	2 / t12f7 8/12	- - - -
JR z,d	28 d	2 / t12f7 8/12	- - - -
LD (addr),A	32 dr ad / EA dr ad	3 / 13	- - - -
LD (addr),BC	ED 43 dr ad	4 / 20 24	- - - -
LD (addr),DE	ED 53 dr ad	4 / 20 24	- - - -
LD (addr),HL	22 dr ad	3 / 16 24	- - - -
LD (addr),HL	ED 63 dr ad	4 / 20 24	- - - -
LD (addr),IX	DD 22 dr ad	4 / 20 24	- - - -
LD (addr),IY	FD 22 dr ad	4 / 20 24	- - - -
LD (addr),SP	ED 73 dr ad / 08 dr ad	4 / 20	- - - -
LD (BC),A	2	1 / 7	- - - -
LD (DE),A	12	1 / 7	- - - -
LD (HL),A	77	1 / 7	- - - -
LD (HL),B	70	1 / 7	- - - -
LD (HL),C	71	1 / 7	- - - -
LD (HL),D	72	1 / 7	- - - -
LD (HL),E	73	1 / 7	- - - -
LD (HL),H	74	1 / 7	- - - -
LD (HL),L	75	1 / 7	- - - -
LD (HL),n	36 n	2 / 10	- - - -
LD ($FF00+C),A	E2	2 / 8	- - - -
LD ($FF00+n) , A	E0 n	2 / 12	- - - -
LD (IX+d),A	DD 77 d	3 / 19	- - - -
LD (IX+d),B	DD 70 d	3 / 19	- - - -
LD (IX+d),C	DD 71 d	3 / 19	- - - -
LD (IX+d),D	DD 72 d	3 / 19	- - - -
LD (IX+d),E	DD 73 d	3 / 19	- - - -
LD (IX+d),H	DD 71 d	3 / 19	- - - -
LD (IX+d),L	DD 75 d	3 / 19	- - - -
LD (IX+d),n	DD 36d n	4 / 19	- - - -

Instruction	Opcodes	B / T	Flags
LD (IY+d),A	FD 77 d	3 / 19	- - - -
LD (IY+d),B	FD 70 d	3 / 19	- - - -
LD (IY+d),C	FD 71 d	3 / 19	- - - -
LD (IY+d),D	FD 72 d	3 / 19	- - - -
LD (IY+d),E	FD 73 d	3 / 19	- - - -
LD (IY+d),H	FD 74 d	3 / 19	- - - -
LD (IY+d),L	FD 75 d	3 / 19	- - - -
LD (IY+d),n	FD 36 d n	4 / 19	- - - -
LD A,(addr)	3A dr ad / F/A dr ad	3 / 16	- - - -
LD A,(BC)	0A	1 / 7 8	- - - -
LD A,(DE)	1A	1 / 7 8	- - - -
LD A,(HL)	7E	1 / 7 8	- - - -
LD A,(IX+d)	DD 7E d	3 / 19	- - - -
LD A,(IY+d)	FD 7E d	3 / 19	- - - -
LD A,A	7F	1 / 4	- - - -
LD A,B	78	1 / 4	- - - -
LD A,C	79	1 / 4	- - - -
LD A,D	7A	1 / 4	- - - -
LD A,E	7B	1 / 4	- - - -
LD A,H	7C	1 / 4	- - - -
LD A,IXH	DD 7C	2 / 8	- - - -
LD A,IYH	FD 7C	2 / 8	- - - -
LD A,I	ED 57	2 / 9	- z i -
LD A,L	7D	1 / 4	- - - -
LD A,IXL	DD 7D	2 / 8	- - - -
LD A,IYL	FD 7D	2 / 8	- - - -
LD A,n	3E n	2 / 7 8	- - - -
LD A, ($FF00+n)	F0 n	2 / 12	- - - -
LD A,($FF00+C)	F2	1 / 8	- - - -
LD A,R	ED 5F	2 / 9	- z i -
LD B,(HL)	46	1 / 7	- - - -
LD B,(IX+d)	DD 46 d	3 / 19	- - - -
LD B,(IY+d)	FD 46 d	3 / 19	- - - -
LD B,A	47	1 / 4	- - - -
LD B,B	40	1 / 4	- - - -
LD B,C	41	1 / 4	- - - -
LD B,D	42	1 / 4	- - - -
LD B,E	43	1 / 4	- - - -
LD B,H	44	1 / 4	- - - -
LD B,IXH	DD 44	2 / 8	- - - -
LD B,IYH	FD 44	2 / 8	- - - -
LD B,L	45	1 / 4	- - - -
LD B,IXL	DD 45	2 / 8	- - - -
LD B,IYL	FD 45	2 / 8	- - - -
LD B,n	06 n	2 / 7 8	- - - -
LD BC,(addr)	ED 4B dr ad	4 / 20	- - - -
LD BC,hilo	01 lo hi	3 / 10 12	- - - -
LD C,(HL)	4E	1 / 7	- - - -
LD C,(IX+d)	DD 4E d	3 / 19	- - - -
LD C,(IY+d)	DD 4E d	3 / 19	- - - -
LD C,A	4F	1 / 4	- - - -
LD C,B	48	1 / 4	- - - -
LD C,C	49	1 / 1	- - - -
LD C,D	4A	1 / 1	- - - -
LD C,E	4B	1 / 4	- - - -
LD C,H	4C	1 / 4	- - - -
LD C,IXH	DD 4C	2 / 8	- - - -
LD C,IYH	FD 4C	2 / 8	- - - -
LD C,L	4D	1 / 4	- - - -
LD C,IXL	DD 4D	2 / 8	- - - -
LD C,IYL	FD 4D	2 / 8	- - - -
LD C,n	0E n	2 / 7 8	- - - -
LD D,(HL)	56	1 / 7	- - - -
LD D,(IX+d)	DD 56 d	3 / 19	- - - -
LD D,(IY+d)	FD 56 d	3 / 19	- - - -
LD D,A	57	1 / 4	- - - -
LD D,B	50	1 / 4	- - - -
LD D,C	51	1 / 4	- - - -
LD D,D	52	1 / 4	- - - -
LD D,E	53	1 / 4	- - - -
LD D,H	54	1 / 4	- - - -
LD D,IXH	DD 54	2 / 8	- - - -
LD D,IYH	FD 54	2 / 8	- - - -
LD D,L	55	1 / 4	- - - -
LD D,IXL	DD 55	2 / 8	- - - -
LD D,IYL	FD 55	2 / 8	- - - -
LD D,n	16 n	2 / 7 8	- - - -
LD DE,(addr)	ED 5B dr ad	4 / 20	- - - -
LD DE,hilo	11 lo hi	3 / 10 12	- - - -
LD E,(HL)	5E	1 / 7	- - - -
LD E,(IX+d)	DD 5E d	3 / 19	- - - -
LD E,(IY+d)	FD 5E d	3 / 19	- - - -
LD E,A	5F	1 / 4	- - - -
LD E,B	58	1 / 4	- - - -
LD E,C	59	1 / 4	- - - -
LD E,D	5A	1 / 4	- - - -
LD E,E	5B	1 / 4	- - - -
LD E,H	5C	1 / 4	- - - -
LD E,IXH	DD 5C	2 / 8	- - - -
LD E,IYH	FD 5C	2 / 8	- - - -
LD E,L	5D	1 / 4	- - - -
LD E,IXL	DD 5D	2 / 8	- - - -
LD E,IYL	FD 5D	2 / 8	- - - -
LD E,n	1E n	2 / 7 8	- - - -
LD H,(HL)	66	1 / 7	- - - -
LD H,(IX+d)	DD 66 d	3 / 19	- - - -
LD H,(IY+d)	FD 66 d	3 / 19	- - - -
LD H,A	67	1 / 4	- - - -
LD H,B	60	1 / 4	- - - -
LD H,C	61	1 / 4	- - - -
LD H,D	62	1 / 4	- - - -
LD H,E	63	1 / 4	- - - -
LD H,H	64	1 / 4	- - - -
LD H,L	65	1 / 4	- - - -
LD H,n	26 n	2 / 7 8	- - - -
LD IXH,A	DD 67	2 / 8	- - - -
LD IXH,B	DD 60	2 / 8	- - - -
LD IXH,C	DD 61	2 / 8	- - - -
LD IXH,D	DD 62	2 / 8	- - - -
LD IXH,E	DD 63	2 / 8	- - - -
LD IXH,IXH	DD 64	2 / 8	- - - -
LD IXH,IXL	DD 65	2 / 8	- - - -
LD IXH,n	DD 26 n	3 / 11	- - - -
LD IYH,A	FD 67	2 / 8	- - - -
LD IYH,B	FD 60	2 / 8	- - - -
LD IYH,C	FD 61	2 / 8	- - - -
LD IYH,D	FD 62	2 / 8	- - - -
LD IYH,E	FD 63	2 / 8	- - - -
LD IYH,IYH	FD 64	2 / 8	- - - -
LD IYH,IYL	FD 65	2 / 8	- - - -
LD IYH,n	FD 26 n	3 / 11	- - - -
LD HL,(addr)	2A dr ad	3 / 16	- - - -
LD HL,(addr)	ED 6B dr ad	4 / 20	- - - -
LD HL,hilo	21 lo hi	3 / 10 12	- - - -
LD HL,SP+n	F8 n	2 / 12	- - - -
LD I,A	ED 47	2 / 9	- - - -
LD IX,(addr)	DD 2A dr ad	4 / 20	- - - -
LD IX,hilo	DD 21 lo hi	4 / 14	- - - -
LD IY,(addr)	FD 2A dr ad	4 / 20	- - - -
LD IY,hilo	FD 21 lo hi	4 / 14	- - - -
LD L,(HL)	6E	1 / 7	- - - -
LD L,(IX+d)	DD 6E d	3 / 19	- - - -
LD L,(IY+d)	FD 6E d	3 / 19	- - - -
LD L,A	6F	1 / 4	- - - -
LD L,B	68	1 / 4	- - - -
LD L,C	69	1 / 4	- - - -
LD L,D	6A	1 / 4	- - - -
LD L,E	6B	1 / 4	- - - -
LD L,H	6C	1 / 4	- - - -
LD L,L	6D	1 / 4	- - - -
LD L,n	2E n	2 / 7	- - - -

Instruction	Opcodes	B / T	Flags
LD IXL,A	DD 6F	2 / 8	- - - -
LD IXL,B	DD 68	2 / 8	- - - -
LD IXL,C	DD 69	2 / 8	- - - -
LD IXL,D	DD 6A	2 / 8	- - - -
LD IXL,E	DD 6B	2 / 8	- - - -
LD IXL,IXH	DD 6C	2 / 8	- - - -
LD IXL,IXL	DD 6D	2 / 8	- - - -
LD IXL,n	DD 2E n	3 / 11	- - - -
LD IYL,A	FD 6F	2 / 8	- - - -
LD IYL,B	FD 68	2 / 8	- - - -
LD IYL,C	FD 69	2 / 8	- - - -
LD IYL,D	FD 6A	2 / 8	- - - -
LD IYL,E	FD 6B	2 / 8	- - - -
LD IYL,IYH	FD 6C	2 / 8	- - - -
LD IYL,IYL	FD 6D	2 / 8	- - - -
LD IYL,n	FD 2En	3 / 11	- - - -
LD R,A	ED 4F	2 / 9	- - - -
LD SP,(addr)	ED 7B dr ad	4 / 20	- - - -
LD SP,hilo	31 lo hi	3 / 10	- - - -
LD SP,HL	F9	1 / 6	- - - -
LD SP,IX	DD F9	2 / 10	- - - -
LD SP,IY	FD F9	2 / 10	- - - -
LDD	ED A8	2 / 16	- - BC -
LDDR	ED B8	2 / z16nz21	- - - -
LDI A,(HL)	2A	2 / 8	- - - -
LDI (HL),A	22	2 / 8	- - - -
LDD A,(HL)	32	2 / 8	- - - -
LDD (HL),A	3A	2 / 8	- - - -
LDI	ED A0	2 / 16	- - BC -
LDIR	ED B0	2 / zl6nz21	- - - -
NEG	ED 44	2 / 8	- z A80 A0
NOP	0	1 / 4	- - - -
OR (HL)	B6	1 / 7	- z P -
OR (IX+d)	DD B6 d	3 / 19	- z p -
OR (IY+d)	FD B6 d	3 / 19	- z p -
OR A	B7	1 / 4	- z p -
OR B	B0	1 / 4	- z p -
OR C	B1	1 / 4	- z p -
OR D	B2	1 / 4	- z p -
OR E	B3	1 / 4	- z p -
OR H	B4	1 / 4	- z p -
OR IXH	DD B4	2 / 8	- z p -
OR IYH	FD B4	2 / 8	- z p -
OR L	B5	1 / 4	- z p -
OR IXL	DD B5	2 / 8	- z p -
OR IYL	FD B5	2 / 8	- z p -
OR n	F6 n	2 / 7	- z p -
OTDR	ED BB	2 / z16nz21	? - ? -
OTIR	ED B3	2 / zl6nz21	? I ? -
OUT (C),A	ED 79	2 / 12 16	- - - -
OUT (C),B	ED 41	2 / 12 16	- - - -
OUT (C),C	ED 49	2 / 12 16	- - - -
OUT (C),D	ED 51	2 / 12 16	- - - -
OUT (C),E	ED 59	2 / 12 16	- - - -
OUT (C),H	ED 61	2 / 12 16	- - - -
OUT (C),L	ED 69	2 / 12 16	- - - -
OUT (n),A	D3 n	2 / 11 12	- - - -
OUTD	ED AB	2 / 16 25	? <>B ? -
OUTI	ED A3	2 / 16 25	? <>B ? -
POP AF	F1	1 / 10	Popped
POP BC	C1	1 / 10	- - - -
POP DE	D1	1 / 10	- - - -
POP HL	E1	1 / 10	- - - -
POP IX	DD E1	2 / 14	- - - -
POP IY	FD E1	2 / 14	- - - -
PUSH AF	F5	1 / 11	- - - -
PUSH BC	C5	1 / 11	- - - -
PUSH DE	D5	1 / 11	- - - -
PUSH HL	E5	1 / 11	- - - -
PUSH IX	DD E5	2 / 15	- - - -
PUSH IY	FD E5	2 / 15	- - - -
RES 0,(HL)	CB 86	2 / 15	- - - -
RES 0,(IX+d)	DD CB d 86	4 / 23	- - - -
RES 0,(IY+d)	FD CB d 86	4 / 23	- - - -
RES 0,A	CB 87	2 / 8	- - - -
RES 0,B	CB 80	2 / 8	- - - -
RES 0,C	CB 81	2 / 8	- - - -
RES 0,D	CB 82	2 / 8	- - - -
RES 0,E	CB 83	2 / 8	- - - -
RES 0,H	CB 81	2 / 8	- - - -
RES 0,L	CB 85	2 / 8	- - - -
RES 1,(HL)	CB 8E	2 / 15	- - - -
RES 1,(IX+d)	DD CB d 8E	4 / 23	- - - -
RES 1,(IY+d)	FD CB d 8E	4 / 23	- - - -
RES 1,A	CB 8F	2 / 8	- - - -
RES 1,B	CB 88	2 / 8	- - - -
RES 1,C	CB 89	2 / 8	- - - -
RES 1,D	CB 8A	2 / 8	- - - -
RES 1,E	CB 8B	2 / 8	- - - -
RES 1,H	CB 8C	2 / 8	- - - -
RES 1,L	CB 8D	2 / 8	- - - -
RES 2,(HL)	CB 96	2 / 15	- - - -
RES 2,(IX+d)	DD CB d 96	4 / 23	- - - -
RES 2,(IY+d)	FD CB d 96	4 / 23	- - - -
RES 2,A	CB 97	2 / 8	- - - -
RES 2,B	CB 90	2 / 8	- - - -
RES 2,C	CB 91	2 / 8	- - - -
RES 2,D	CB 92	2 / 8	- - - -
RES 2,E	CB 93	2 / 8	- - - -
RES 2,H	CB 94	2 / 8	- - - -
RES 2,L	CB 95	2 / 8	- - - -
RES 3,(HL)	CB 9E	2 / 15	- - - -
RES 3,(IX+d)	DD CB d 9E	4 / 23	- - - -
RES 3,(IY+d)	FD CB d 9E	4 / 23	- - - -
RES 3,A	CB 9F	2 / 8	- - - -
RES 3,B	CB 98	2 / 8	- - - -
RES 3,C	CB 99	2 / 8	- - - -
RES 3,D	CB 9A	2 / 8	- - - -
RES 3,E	CB 9B	2 / 8	- - - -
RES 3,H	CB 9C	2 / 8	- - - -
RES 3,L	CB 9D	2 / 8	- - - -
RES 4,(HL)	CB A6	2 / 15	- - - -
RES 4,(IX+d)	DD CB d A6	4 / 23	- - - -
RES 4,(IY+d)	FD CB d A6	4 / 23	- - - -
RES 4,A	CB A7	2 / 8	- - - -
RES 4,B	CB A0	2 / 8	- - - -
RES 4,C	CB A1	2 / 8	- - - -
RES 4,D	CB A2	2 / 8	- - - -
RES 4,E	CB A3	2 / 8	- - - -
RES 4,H	CB A4	2 / 8	- - - -
RES 4,L	CB A5	2 / 8	- - - -
RES 5,(HL)	CB AE	2 / 15	- - - -
RES 5,(IX+d)	DD CB d AE	4 / 23	- - - -
RES 5,(IY+d)	FD CB d AE	4 / 23	- - - -
RES 5,A	CB AF	2 / 8	- - - -
RES 5,B	CB A8	2 / 8	- - - -
RES 5,C	CB A9	2 / 8	- - - -
RES 5,D	CB AA	2 / 8	- - - -
RES 5,E	CB AB	2 / 8	- - - -
RES 5,H	CB AC	2 / 8	- - - -
RES 5,L	CB AD	2 / 8	- - - -
RES 6,(HL)	CB B6	2 / 15	- - - -
RES 6,(IX+d)	DD CB d B6	4 / 23	- - - -
RES 6,(IY+d)	FD CB d B6	4 / 23	- - - -
RES 6,A	CB B7	2 / 8	- - - -
RES 6,B	CB B0	2 / 8	- - - -
RES 6,C	CB B1	2 / 8	- - - -
RES 6,D	CB B2	2 / 8	- - - -
RES 6,E	CB B3	2 / 8	- - - -
RES 6,H	CB B4	2 / 8	- - - -
RES 6,L	CB B5	2 / 8	- - - -

Instruction	Opcodes	B / T	Flags
RES 7,(HL)	CB BE	2 / 15	- - - -
RES 7,(IX+d)	DD CB d BE	4 / 23	- - - -
RES 7,(IY+d)	FD CB d BE	4 / 23	- - - -
RES 7,A	CB BF	2 / 8	- - - -
RES 7,B	CB B8	2 / 8	- - - -
RES 7,C	CB B9	2 / 8	- - - -
RES 7,D	CB BA	2 / 8	- - - -
RES 7,E	CB BB	2 / 8	- - - -
RES 7,H	CB BC	2 / 8	- - - -
RES 7,L	CB BD	2 / 8	- - - -
RET	C9	1 / 10 12	- - - -
RET C	D8	1 / t11f8 8/16	- - - -
RET M	F8	1 / t11f8 8/16	- - - -
RET NC	D0	1 / t11f8 8/16	- - - -
RET NZ	C0	1 / t11f8 8/16	- - - -
RET P	F0	1 / t11f8 8/16	- - - -
RET PE	E8	1 / t11f8 8/16	- - - -
RET PO	E0	1 / t11f8 8/16	- - - -
RET Z	C8	1 / t11f8 8/16	- - - -
RETI	ED 4D / D9	1 / 8	- - - -
RETN	ED 45	2 / 14	- - - -
RL (HL)	CB 16	2 / 15	- z p r7
RL (IX+d)	DD CB d 16	4 / 23	- z p r7
RL (IY+d)	FD CB d 16	4 / 23	- z p r7
RL A	CB 17	2 / 8	- z p r7
RL B	CB 10	2 / 8	- z p r7
RL C	CB 11	2 / 8	- z p r7
RL D	CB 12	2 / 8	- z p r7
RL E	CB 13	2 / 8	- z p r7
RL H	CB 14	2 / 8	- z p r7
RL L	CB 15	2 / 8	- z p r7
RLA	17	1 / 4	- - - r7
RLC (HL)	CB 06	2 / 15	- z p r7
RLC (IX+d)	DD CB d 06	4 / 23	- z p r7
RLC (IY+d)	FD CB d 06	4 / 23	- z p r7
RLC A	CB 07	2 / 8	- z p r7
RLC B	CB 00	2 / 8	- z p r7
RLC C	CB 01	2 / 8	- z p r7
RLC D	CB 02	2 / 8	- z p r7
RLC E	CB 03	2 / 8	- z p r7
RLC H	CB 04	2 / 8	- z p r7
RLC L	CB 05	2 / 8	- z p r7
RLCA	7	1 / 4	- - - r7
RLD	ED 6F	2 / 18	- z p -
RR (HL)	CB 1E	2 / 15	- z p r0
RR (IX+d)	DD CB d 1E	4 / 23	- z p r0
RR (IY+d)	FD CB d 1E	4 / 23	- z p r0
RR A	CB 1F	2 / 8	- z p r0
RR B	CB 18	2 / 8	- z p r0
RR C	CB 19	2 / 8	- z p r0
RR D	CB 1A	2 / 8	- z p r0
RR E	CB 1B	2 / 8	- z p r0
RR H	CB 1C	2 / 8	- z p r0
RR L	CB 1D	2 / 8	- z p r0
RRA	1F	1 / 4	- - - r0
RRC (HL)	CB 0E	2 / 15	- z p r0
RRC (IX+d)	DD CB d 0E	4 / 23	- z p r0
RRC (IY+d)	FD CB d 0E	4 / 23	- z p r0
RRC A	CB 0F	2 / 8	- z p r0
RRC B	CB 08	2 / 8	- z p r0
RRC C	CB 09	2 / 8	- z p r0
RRC D	CB 0A	2 / 8	- z p r0
RRC E	CB 0B	2 / 8	- z p r0
RRC H	CB 0C	2 / 8	- z p r0
RRC L	CB 0D	2 / 8	- z p r0
RRCA	0F	1 / 4	- - - r0
RRD	ED 67	2 / 18	- z p -
RST 0	C7	1 / 11 16	- - - -
RST 8 (1)	CF	1 / 11 16	- - - -
RST 16 (2)	D7	1 / 11 16	- - - -
RST 24 (3)	DF	1 / 11 16	- - - -
RST 32 (4)	E7	1 / 11 16	- - - -
RST 40 (5)	EF	1 / 11 16	- - - -
RST 48 (6)	F7	1 / 11 16	- - - -
RST 56 (7)	FF	1 / 11 16	- - - -
SBC A,(HL)	9E	1 / 7	- z v b
SBC A,(IX+d)	DD 9Ed	3 / 19	- z v b
SBC A,(IY+d)	FD 9Ed	3 / 19	- z v b
SBC A,A	9F	1 / 4	- z v b
SBC A,B	98	1 / 4	- z v b
SBC A,C	99	1 / 4	- z v b
SBC A,D	9A	1 / 4	- z v b
SBC A,E	9B	1 / 4	- z v b
SBC A,H	9C	1 / 4	- z v b
SBC A,IXH	DD 9C	2 / 8	- z v b
SBC A,IYH	FD 9C	2 / 8	- z v b
SBC A,L	9D	1 / 4	- z v b
SBC A,IXL	DD 9D	2 / 8	- z v b
SBC A,IYL	FD 9D	2 / 8	- z v b
SBC A,n	DE n	2 / 7	- z v b
SBC HL,BC	ED 42	2 / 15	- z v b
SBC HL,DE	ED 52	2 / 15	- z v b
SBC HL,HL	ED 62	2 / 15	- z v b
SBC HL,SP	ED 72	2 / 15	- z v b
SCF	37	1 / 4	- - - -
SET 0,(HL)	CB C6	2 / 15	- - - -
SET 0,(IX+d)	DD CB d C6	4 / 23	- - - -
SET 0,(IY+d)	FD CB d C6	4 / 23	- - - -
SET 0,A	CB C7	2 / 8	- - - -
SET 0,B	CB C0	2 / 8	- - - -
SET 0,C	CB C1	2 / 8	- - - -
SET 0,D	CB C2	2 / 8	- - - -
SET 0,E	CB C3	2 / 8	- - - -
SET 0,H	CB C4	2 / 8	- - - -
SET 0,L	CB C5	2 / 8	- - - -
SET 1,(HL)	CB CE	2 / 15	- - - -
SET 1,(IX+d)	DD CB d CE	4 / 23	- - - -
SET 1,(IY+d)	FD CB d CE	4 / 23	- - - -
SET 1,A	CB CF	2 / 8	- - - -
SET 1,B	CB C8	2 / 8	- - - -
SET 1,C	CB C9	2 / 8	- - - -
SET 1,D	CB CA	2 / 8	- - - -
SET 1,E	CB CB	2 / 8	- - - -
SET 1,H	CB CC	2 / 8	- - - -
SET 1,L	CB CD	2 / 8	- - - -
SET 2,(HL)	CB D6	2 / 15	- - - -
SET 2,(IX+d)	DD CB d D6	4 / 23	- - - -
SET 2,(IY+d)	FD CB d D6	4 / 23	- - - -
SET 2,A	CB D7	2 / 8	- - - -
SET 2,B	CB D0	2 / 8	- - - -
SET 2,C	CB D1	2 / 8	- - - -
SET 2,D	CB D2	2 / 8	- - - -
SET 2,E	CB D3	2 / 8	- - - -
SET 2,H	CB D4	2 / 8	- - - -
SET 2,L	CB D5	2 / 8	- - - -
SET 3,(HL)	CB DE	2 / 15	- - - -
SET 3,(IX+d)	DD CB d DE	4 / 23	- - - -
SET 3,(IY+d)	FD CB d DE	4 / 23	- - - -
SET 3,A	CB DF	2 / 8	- - - -
SET 3,B	CB D8	2 / 8	- - - -
SET 3,C	CB D9	2 / 8	- - - -
SET 3,D	CB DA	2 / 8	- - - -
SET 3,E	CB DB	2 / 8	- - - -
SET 3,H	CB DC	2 / 8	- - - -
SET 3,L	CB DD	2 / 8	- - - -

Alternate instructions with the same meaning:

LD ($FF00+n) , A	LDH (n),A
LD A, ($FF00+n)	LDH A,(n)
LDI (HL),A	LD (HLI),A or LD (HL+),A
LDI A,(HL)	LD A,(HLI) or LD A,(HL+)
LDD (HL),A	LD (HLD),A or LD (HL-),A
LDD A,(HL)	LD A,(HL-) or LD A,(HLD)
LD A,(C)	LD A,($FF00+C)
LD (C),A	LD ($FF00+C),A
LD HL,SP+n	LDHL SP,n ..

Instruction	Opcodes	B / T	Flags
SET 4,(HL)	CB E6	2 / 15	- - - -
SET 4,(IX+d)	DD CB d E6	4 / 23	- - - -
SET 4,(IY+d)	FD CB d E6	4 / 23	- - - -
SET 4,A	CB E7	2 / 8	- - - -
SET 4,B	CB E0	2 / 8	- - - -
SET 4,C	CB E1	2 / 8	- - - -
SET 4,D	CB E2	2 / 8	- - - -
SET 4,E	CB E3	2 / 8	- - - -
SET 4,H	CB E4	2 / 8	- - - -
SET 4,L	CB E5	2 / 8	- - - -
SET 5,(HL)	CB EE	2 / 15	- - - -
SET 5,(IX+d)	DD CB d EE	4 / 23	- - - -
SET 5,(IY+d)	FD CB d EE	4 / 23	- - - -
SET 5,A	CB EF	2 / 8	- - - -
SET 5,B	CB E8	2 / 8	- - - -
SET 5,C	CB E9	2 / 8	- - - -
SET 5,D	CB EA	2 / 8	- - - -
SET 5,E	CB EB	2 / 8	- - - -
SET 5,H	CB EC	2 / 8	- - - -
SET 5,L	CB ED	2 / 8	- - - -
SET 6,(HL)	CB F6	2 / 15	- - - -
SET 6,(IX+d)	DD CB d F6	4 / 23	- - - -
SET 6,(IY+d)	FD CB d F6	4 / 23	- - - -
SET 6,A	CB F7	2 / 8	- - - -
SET 6,B	CB F0	2 / 8	- - - -
SET 6,C	CB F1	2 / 8	- - - -
SET 6,D	CB F2	2 / 8	- - - -
SET 6,E	CB F3	2 / 8	- - - -
SET 6,H	CB F4	2 / 8	- - - -
SET 6,L	CB F5	2 / 8	- - - -
SET 7,(HL)	CB FE	2 / 15	- - - -
SET 7,(IX+d)	DD CB d FE	4 / 23	- - - -
SET 7,(IY+d)	FD CB d FE	4 / 23	- - - -
SET 7,A	CB FF	2 / 8	- - - -
SET 7,B	CB F8	2 / 8	- - - -
SET 7,C	CB F9	2 / 8	- - - -
SET 7,D	CB FA	2 / 8	- - - -
SET 7,E	CB FB	2 / 8	- - - -
SET 7,H	CB FC	2 / 8	- - - -
SET 7,L	CB FD	2 / 8	- - - -
SLA (HL)	CB 26	2 / 15	- z p r7
SLA (IX+d)	DD CB d 26	4 / 23	- z p r7
SLA (IY+d)	FD CB d 26	4 / 23	- z p r7
SLA A	CB 27	2 / 8	- z p r7
SLA B	CB 20	2 / 8	- z p r7
SLA C	CB 21	2 / 8	- z p r7
SLA D	CB 22	2 / 8	- z p r7
SLA E	CB 23	2 / 8	- z p r7
SLA H	CB 24	2 / 8	- z p r7
SLA L	CB 25	2 / 8	- z p r7
SLL (HL)	CB 36	2 / 15	- z p r7
SLL (IX+d)	DD CB d 36	4 / 23	- z p r7
SLL (IY+d)	FD CB d 36	4 / 23	- z p r7
SLL A	CB 37	2 / 8	- z p r7
SLL B	CB 30	2 / 8	- z p r7
SLL C	CB 31	2 / 8	- z p r7
SLL D	CB 32	2 / 8	- z p r7
SLL E	CB 33	2 / 8	- z p r7
SLL H	CB 34	2 / 8	- z p r7
SLL L	CB 35	2 / 8	- z p r7
SRA (HL)	CB 2E	2 / 15	- z p r0
SRA (IX+d)	DD CB d 2E	4 / 23	- z p r0
SRA (IY+d)	FD CB d 2E	4 / 23	- z p r0
SRA A	CB 2F	2 / 8	- z p r0
SRA B	CB 28	2 / 8	- z p r0
SRA C	CB 29	2 / 8	- z p r0
SRA D	CB 2A	2 / 8	- z p r0
SRA E	CB 2B	2 / 8	- z p r0
SRA H	CB 2C	2 / 8	- z p r0
SRA L	CB 2D	2 / 8	- z p r0
SRL (HL)	CB 3E	2 / 15	- z p r0
SRL (IX+d)	DD CB d 3E	4 / 23	- z p r0
SRL (IY+d)	FD CB d 3E	4 / 23	- z p r0
SRL A	CB 3F	2 / 8	- z p r0
SRL B	CB 38	2 / 8	- z p r0
SRL C	CB 39	2 / 8	- z p r0
SRL D	CB 3A	2 / 8	- z p r0
SRL E	CB 3B	2 / 8	- z p r0
SRL H	CB 3C	2 / 8	- z p r0
SRL L	CB 3D	2 / 8	- z p r0
STOP	10 00	2 / 4	- - - -
SUB (HL)	96	1 / 7	- z v b
SUB (IX+d)	DD 96 d	3 / 19	- z v b
SUB (IY+d)	FD 96 d	3 / 19	- z v b
SUB A	97	1 / 4	- z v b
SUB B	90	1 / 4	- z v b
SUB C	91	1 / 4	- z v b
SUB D	92	1 / 4	- z v b
SUB E	93	1 / 4	- z v b
SUB H	94	1 / 4	- z v b
SUB IXH	DD AC	2 / 8	- z v b
SUB IYH	FD AC	2 / 8	- z v b
SUB L	95	1 / 4	- z v b
SUB IXL	DD AD	2 / 8	- z v b
SUB IYL	FD AD	2 / 8	- z v b
SUB n	D6 n	2 / 7	- z v b
SWAP A	CB 37	2 / 8	- z v z
SWAP B	CB 30	2 / 8	- z v z
SWAP C	CB 31	2 / 8	- z v z
SWAP D	CB 32	2 / 8	- z v z
SWAP E	CB 33	2 / 8	- z v z
SWAP H	CB 34	2 / 8	- z v z
SWAP L	CB 35	2 / 8	- z v z
SWAP (HL)	CB 36	2 / 16	- z v z
XOR (HL)	AE	1 / 7	- z p -
XOR (IX+d)	DD AC d	3 / 19	- z p -
XOR (IY+d)	FD AC d	3 / 19	- z p -
XOR A	AF	1 / 4	- z p -
XOR B	A8	1 / 4	- z p -
XOR C	A9	1 / 4	- z p -
XOR D	AA	1 / 4	- z p -
XOR E	AB	1 / 4	- z p -
XOR H	AC	1 / 4	- z p -
XOR IXH	DD AC	2 / 8	- z p -
XOR IYH	FD AD	2 / 8	- z p -
XOR L	AD	1 / 4	- z p -
XOR IXL	DD AC	2 / 8	- z p -
XOR IYL	FD AD	2 / 8	- z p -
XOR n	EE n	2 / 7	- z p -

BUG: If you are using sprites then you should not use the following commands (INC rr / DEC rr) when their register contents are in the range $fe00-$feff . If you don't follow this rule, sprite trashing the form of sprite "blink" will randomly affect your sprites BUG:on the GBZ80, HALT when interrupts are disabled will not lock the CPU, however the instruction immediately following the HALT instruction is "skipped" ,so put a NOP after the halt instruction If you don't follow this rule, sprite trashing the form of sprite "blink" will randomly affect your sprites BUG:on the GBZ80, HALT when interrupts are disabled will not lock the CPU, however the instruction immediately following the HALT instruction is "skipped" ,so put a NOP after the halt instruction

Black: GBZ80 & Z80
Blue: Z80 only
Red: GBZ80 only
Purple: Cpc Timings